ENGINEERING NOTEBOOK

CONFIDENTIAL

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ENGINEERING NOTEBOOK

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2. Complete each sheet in its entirety, but start a new sheet on every new day that you wish to record information.
3. Date and sign each log sheet.
4. All log sheets containing information that might have particular significance must be signed and dated by one witness who reads the sheet and understands its contents.
   NOTE: If there are co-inventors, both should sign in the area marked *WRITER,* and a third party is required to sign as witness.
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1. Use black ink. Do not use blue ink or pencil; it is difficult to reproduce.
2. Do not try to erase. If revisions or changes are necessary, cross out and rewrite. See item 8 of instructions.
3. Clarity is essential but precision drawings are not required; therefore, free-hand sketches are acceptable.

Book No. 7682 *Assigned to* Joe Decuir

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BOOKS ASSIGNED BY
ATARI BOSTON OFFICE

ATARI ENGINEERING LOG SHEET

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GAME OR PROJECT

STELLA *

ADJUSTING TO THIS NOTE BOOK COULD BE A PROBLEM. EVERYBODY HAS HIS/HER HABITS, AND MAJOR ADJUSTMENTS ARE DIFFICULT.

ON APRIL 1, 1976 I STARTED A NOTEBOOK. RETROACTIVELY NUMBERED "13" ON 2FEB77. VERY LITTLE OF MY DESIGN WORK, OR IDEAS, PARTICULARLY FOR PROGRAMS, IS CONTAINED IN THAT BOOK. I HABITUALLY WORK ON GREEN "ENGINEERING PADS". ANYTHING WORTH SAVING WINDS UP IN BINDERS.

I SUSPECT THAT THE DOMINANT VALUE OF THIS BOOK IS LEGAL DOCUMENTATION OF PROPRIETARY IDEAS. MY GREEN SHEETS SERVE FINE FOR GETTING THE WORK DONE, BUT I DOUBT THAT THEY WILL STAND UP IN COURT.

ANOTHER FUNCTION OF THIS BOOK MAY BE SO THAT AN "ENGINEERING MANAGER" CAN EVALUATE MY WORK. THIS DOES CONSTITUTE A PROBLEM, SINCE THE LINES OF AUTHORITY HERE ARE NOT CLEAR. I DO WHAT NEEDS TO BE DONE, WITH PRIORITY DETERMINED BY CONSENSUS WITH JAY MINER, LARRY WAGNER, AND BOB BROWN, → AND NILES STROHL, THE STELLA PROJECT ENGINEER WITHIN THE CONSUMER PRODUCT ENGINEER GROUP DOWN THE HALL.

IF MICROELECTRONICS FRAGMENTS IN TO A CHIP DEVELOPMENT GROUP AND A SOFTWARE DEVELOPMENT GROUP, MY ROLE WILL BECOME CONFUSED.

THESE ARE MY THOUGHTS ON WHAT SHOULD GO IN HERE; AND IF ANYONE BESIDES BOB BROWN THINKS HE HAS ANYTHING TO SAY ABOUT IT, HE/SHE SHOULD SPEAK SOON. I CONSIDER DR. BROWN AS MY BOSS.

* NAMED AFTER MY BICYCLE, A STELLA SX-73 10kg bike

GAME OR PROJECT
STELLA

WHAT SHOULD GO IN THIS BOOK:

DAILY SUMMARIES OF IDEAS ABOUT:
- NEW SYSTEM ARCHITECTURES, INCLUDING CHIPS.
- DEVELOPMENT SYSTEM ARCHITECTURES.
- FUNCTIONAL SPECIFICATIONS FOR SOFTWARE:
  - CHIP DIAGNOSTICS
  - BOARD DIAGNOSTICS
  - DEVELOPMENT SYSTEM DIAGNOSTICS.
  - GAME (APPLICATIONS) SOFTWARE.
- SOME INTERNAL SPECIFICATIONS FOR ABOVE SOFTWARE.
- THOUGHTS AND OBSERVATIONS ABOUT OTHER SYSTEMS, CHIPS SETS (EX: SIGNETICS)
- IDEAS FOR GAMES FROM COIN OP

DAILY SUMMARIES OF: PROBLEMS ENCOUNTERED IN DEVELOPMENT SYSTEM WORK.

MAYBE OTHER THINGS, WHEN I THINK OF THEM.

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GAME OR PROJECT
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PADDLE GAME CODE.

TO DATE A 4 PLAYER 2 PADDLE/PLAYER SOCCER GAME HAS BEEN WRITTEN FOR STELLA. I AND ~~S~~BOOB BANERJEE ARE CONVERTING IT TO A 4 PLAYFIELD / 16-32 PADDLE CONFIGURATION SYSTEM OF VERTICAL PADDLE GAMES. THIS GAME SET WILL BE SUBMITTED TO ~~TO~~ THE GROUP FOR PLAY - WRINGING OUT - AND COMMENTS. IT WILL USE BOTH OPTION AND GAME SELECTS.

AFTER COMMENTS IT WILL BE BOILED DOWN INTO A SPECIFIC GAME SET, USING GAME SELECT ONLY.

THEN A SET OF PADDLE GAMES INCORPORATING HORIZONTAL PADDLES, INCLUDING BASKETBALL, QUADRAPONG, AND VOLLEYBALL (REBOUND) WILL BE PURSUED. (I WOULD HOPE THAT MR. BANERJEE GETS TO DO THIS).

I WILL THEN PURSUE BREAK OUT, PIN PONGS (a la ARCENTE), AND A WHEELS GAME FOR SEARS.

AFTER THAT. I DON'T KNOW.

I WILL BE TRAINING NEW ~~MEN~~ PEOPLE AS PROGRAMMERS AND ~~TO~~ FOR HARDWARE SUPPORT.

I WILL HELP JAY, STEVE MAYER, AND KARRY WAGNER TO ARCHITECT A FOLLOW ON TO STELLA.

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WRITER JSCOLLER	DATE 2 FEB 77	WITNESS Greg A. Miller	DATE

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GAME OR PROJECT
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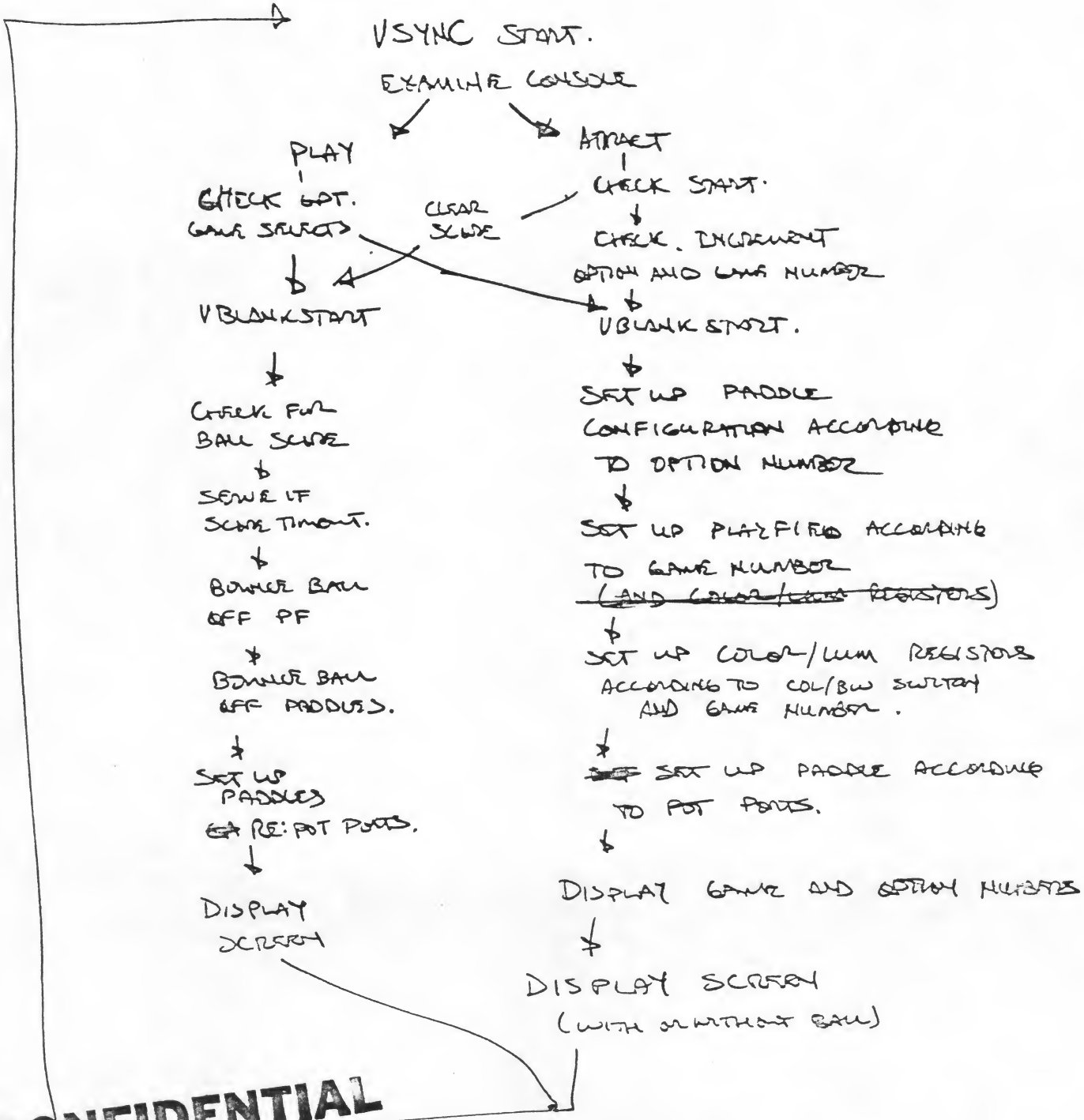
DESIGN OF ~~STAR~~ PADDLE GAME EXEC.



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GAME OR PROJECT
STELLA

3RD, 4th FEBRUARY - WROTE AND DEBUGGED ATTRACT MODE CODE, INSTALLED GAME NUMBER DEPENDANT PLAYFIELD AND COLORS. B/W SWITCH SOFTWARE.

MONDAY & TUESDAY 7th, 8th FEBRUARY
MOST TIME SPENT FIRE FIGHTING.

NILES STROHL DESIGNED AND INSTALLED A MODIFICATION TO KIM DEVELOPMENT SYSTEM THAT MIXES SOUND IN WITH VIDEO → INTO TV SPEAKER. IT WORKS SATISFACTORILY, W/O SERIOUSLY DEGRADING LOW FREQUENCY RESPONSE OF AUDIO.

SOME KINDS OF SERIOUS PROBLEMS ARE OCCURING BETWEEN THE BREADBOARD AND LARRY WAGNER'S PROGRAMS. SOME FAULTS TRACED TO KIM SYSTEM RAMS, BUT THESE ARE INDEPENDANT.

WEDNESDAY, THURSDAY, FRIDAY. 9, 10, 11 FEB.
NUTS & BOLTS STUFF,
GETTING STELLA READY FOR MARKET TESTING.

MONDAY 14FEB MORE OF SAME.

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GAME OR PROJECT
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15 FEB NOTES ON READING ABOUT 6I TANK AND OTHER CHIPS IN THE 6I BOOK

OBJECT RESOLUTION LOOKS COARSE FROM THE SPECS. "8/100" OF SCREEN VS 8/160 FOR STELLA

~~MOTION~~ MOTION SOUNDS FINER. "32 POSITIONS" "32 DIRECTIONS"
VS 16 POSITIONS AND DIRECTIONS FOR STELLA.

~~3~~ 3 FORWARD AND 3 REVERSE SPEEDS
REVERSE SOUNDS USEFUL - BUT I DON'T KNOW ABOUT MULTIPLE SPEEDS - THEY'RE EASY TO DO WITH THE TIME FEATURE

THEY HAVE MINES, AND THEY HAVE BULLET EXPLOSIONS.

SCORING - ~~IS~~ IN 6I - GAME ENDS AT 31.
USE - GAME ENDS AT 10
- WE COULD INCREASE UPPER LIMITS OF SCORE. BUT IT MIGHT JUST INCREASE LENGTH OF GAME

WE DON'T HAVE A GENERAL PURPOSE MICRO PROGRAMMABLE CHIP, TO ~~GENERATE~~ GENERATE SINGLE CHIP GAMES.
MOS TECHNOLOGY'S GAME CHIP, AND ARCUTE ARE BOTH EXAMPLES OF SUCH A DEVICE. WE OUGHT TO CONSIDER SUCH A MACHINE FOR A 1978 PRODUCT.

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FOR EXAMPLE,

WHY NOT LOOK AT THE
MOS TECHNOLOGY 6502 / ATARI TIA
/ 6532 TRIO.

DESIGN A SPECIAL PURPOSE
MACHINE THAT EXECUTES A MICRO CODE -
(PERHAPS IN AN EXTERNAL ROM) WHICH
IS (AT A FLOW CHART LEVEL) SIMILAR TO
THAT EXECUTED BY STELLA PROGRAMS.
— EXCEPT THAT THERE ARE FEWER VARIABLES
- AND MORE SPECIAL PURPOSE INSTRUCTIONS.

EX: RIGHT NOW THE 6502 DRAWS THE
TANK GRAPHICS LINE PAIR BY LINE PAIR

SUPPOSE A MICRO PROGRAMMED MACHINE
HAS A REGISTER FOR OBJECT X VERTICAL
POSITION, AND A REGISTER FOR OBJECT X
DISPLAY. AND AN NXN BIT PATTERN
FOR OBJECT X GRAPHICS.
A SINGLE INSTRUCTION MIGHT
DO A COMPARISON OF VPOS AND LINE COUNT.
AND DECIDE RANGE, AND INDEX TO GRAPHICS.
A SECOND INSTRUCTION WOULD BRANCH ON RANGE.
A THIRD INSTRUCTION WOULD LOAD DISP INTO
GRAPHICS.

PLAYFIELD COULD BE A RESIDENT ROM.

ETC.

WRITER Joe Decuir	DATE 1/27/82	WITNESS [signature]	DATE 2/1/82

GAME OR PROJECT
NEW RECORDS FOR '78 / PADDLE GAMES.

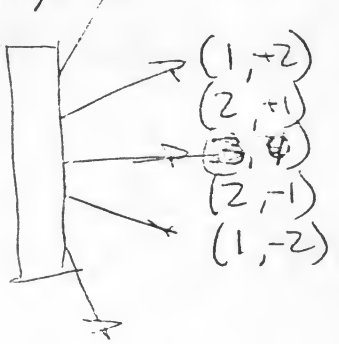
THE BASIC IDEA - I SUPPOSE, IS TO GO FOR THE MIDDLE GROUND BY BUILDING SINGLE CUSTOM (+ MAYBE SEMI RAMS/ROMS) WHICH CAN DO SMALL (40) SET OF GAMES. - TAKE SOME SYSTEM FUNCTIONS AND REPARTITION. INTO ARCADE LIKE SYSTEMS.

BALL / PADDLE INTERACTION ALGORITHMS.

1) SIMPLE. $|HM| = 1$.
SIGN (HM) = FUNCTION OF PLAYER #.
VM = FUNCTION OF IMPACT POINT -2 - +2

2) $|HM| = 1, 2, 3$
# HITS = 0, 1, 2, 3 ⇒ 1
# HITS = 4, 5, 6, 7 ⇒ 2
# HITS ≥ 8 ⇒ 3
SIGN = FUNCTION OF PLAYER #.
VM = FUNCTION OF IMPACT POINT.

3) |HM|, VMS = FUNCTION OF IMPACT POINT.



OR

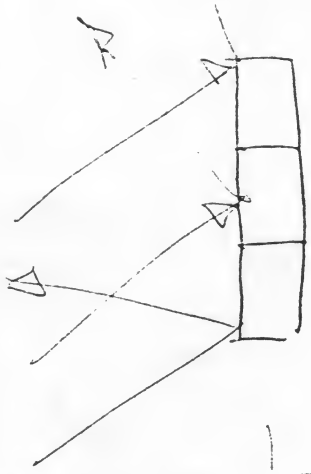
SIGN HM ⇐ PLAYER #.

VM	HM
+2	1
+1	
0	2
-1	
-2	1

GAME OR PROJECT
PADDLE GAMES

4) "ENGLISH"

$(|HM|, VM) = f(|OLD\,HM|, OLD\,VM, IMPACT\,POINT)$



$VM = VM + 1$	$|HM| = |HM| - 1$
$VM = VM$	$|HM| = |HM|$
$VM = VM - 1$	$|HM| = |HM| + 1$

$HM = 1, 2, 3, -1, -2, -3$ $\quad VM =$

	$|HM| =$	$VM =$
1)	HM	f(IMPACT PT) $-2 \le VM \le +2$
2)	f(# OF HITS) $-3 \le HM \le +3$ AND $\neq 0$	f(IMPACT PT) $-2 \le VM \le +2$
3)	f(IMPACT PT)	f(IMPACT PT) $-2 \le VM \le +2$
4)	f(IMPACT PT, HM)	f(IMPACT PT, VM)

AUDIO VOLUME = $|HM| \times 4$.

$$Q2 = |HM| + |VM| \times 2$$

Q2 = FUNCTION OF IMPACT PT.

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GAME OR PROJECT
NEW MACHINES

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IF 11 PINS ARE USED ON A SCREEN MAP TO CONTROL A ~~[illegible]~~ DYNAMIC RAM ~~[illegible]~~ ARRAY. - IT HAS 13 LEFT IN A 28 PIN PACKAGE. AND 29 LEFT IN A 40 PIN.

AS A MINIMUM ADDITO AN EXISTING SYSTEM, IT NEEDS:

2	+5, GRND		
2	OSC IN, ϕ2 IN		
8	Dϕ - D7		
2-3	CHIP SELECTS.	} 8 MINIMUM	
9-10 1	R/W		
3-6	ADDRESS LINES		
21-22	LINES		
~~[illegible]~~	~~[illegible]~~		
1-4	VIDEO OUT	(1 IF PIPED INTO SYSTEM, 4 IF CHROMA/LUM ET)	
22-26			
+11	RAM CONTROL		
33-37	⟹ 40 PINS		

IF THIS IS A STAND ~~ALONE~~ ALONE SYSTEM -

DELETE A CHIP SELECT. ~~AD~~
ADD A COLOR DELAY INPUT. ~~AND A [illegible]~~
ADD A ϕ_0 OUTPUT
ADD A $\overline{IRQ}$ OR RDY OUTPUT
ADD ~~1 or 2~~ ANALOG OUTPUTS.
ADD 1 BLANK OUTPUT

4-5
~~33~~ 37
41-42 !!

WRITER [illegible] | DATE [illegible] | WITNESS [illegible] | DATE 2-10-82

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GAME OR PROJECT

NEW MACHINES

TIA:			6502 INDEPENDENT:	
GND			GND	1
SYN			SYN	2
RDY			RDY or IRQ	3
ϕ_0 OUT			ϕ_0 OUT	4
L1			L1	5
BL			BL (?)	
L2			L2	6
Lϕ			Lϕ (?)	
COL			COL	7
DEL			DEL	8
OSC			OSC	9
AU1			AU1	10
AUϕ				
Dϕ			Dϕ	11
D1			D1	12
D2			D2	13
D3			D3	14
D4			D4	15
D5			D5	16
+5			+5	17
$\overline{CS3}$			~~$\overline{CS3}$~~	
$\overline{CS2}$			$\overline{CS2}$	18
CS1			~~CS1~~	
$\overline{CS\phi}$			$\overline{CS\phi}$	19
R/W			R/W	20
ϕ2 IN			ϕ2 IN	21
A5			{A5, A4} ?	
A4				
A3			A3	22
A2			A2	23
A1			A1	24
Aϕ			Aϕ	25
D6			D6	26
D7			D7	27

40 INPUTS.

27 +11 38

WRITER DSAUR | DATE 1 FEB 77 | WITNESS Jay Miner | DATE 2/17/77

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GAME OR PROJECT
NEW MACHINES

ADD ON CHARACTER CHIP TO TIA

IT COULD FIT INTO THE SAME MEMORY SPACE AS THE TIA:
19 WRITE ADDRESSES FROM (2D TO 3F)

3F
2C
$13_H = 19$

~~[illegible]~~
~~? READ ADDRESSES~~
OR USE ONE CHIP SELECT ON A8
TO DISTINGUISH IF FROM STELLA - GIVING IT
64 R/W ADDRESSES.

COULD USE THE RDY LINE IN PARALLEL WITH TIA FOR RESYNCHRONIZATION - OR HAVE MICRO DO THAT ITSELF W/ TIA.

~~PINS~~
~~+5~~ COULD ENCODE ITS OUTPUT INTO TIA ON ONE OR TWO LINES, OR MIX THEM EXTERNALLY BY WIRED OR ON CHROMA AND LUM LINES.

---

2 +5, GND
2 $\phi 2$, OSC
8 Dϕ - D7
8 } 2 CHIP SELECTS AND 6 ADDRESS LINES AND NO R/W
~~6~~ OR ~~8~~ 10 3 CHIP SELECTS. AND 8 ADDR — 6 ADDRESS LINES AND R/W }
2ϕ - 30

+ VIDEO OUTPUTS
1 - 4 1-2 OR ~~3~~ INTO TIA OR 3-4 VIDEO OUTPUTS
2ϕ - 34 TOTAL PINS.

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GAME OR PROJECT
NEW MACHINES.

SUPPOSE USE 4 WRITE ADDRESSES ONLY.

A1, A0 =

0	CONTROL WORD
1	SHIFT REGISTER DATA - WRITE 20 TIMES.
2	WRITABLE CHARACTER ADDRESS
3	WRITABLE CHARACTER DATA.

PUT IN LOCATIONS $40-7F_H$ REDUNANTLY.

$\overline{CS0}$ = A12
$\overline{CS1}$ = A7
$\overline{CS2}$ = A6
A1 = A1
A0 = A0

5	LINES CS/AD.
2	POWER
2	CLOCKS
8	DATA
17	PINS.
7	PINS FOR OUTPUT.
24	PIN PACKAGE.

EX. 1 LINE INTO TIA. - COLU
OR 1 LINE INTO TIA FOR TURN OFF
3 COLU, 1 CHR, 1 CHDEL.

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GAME OR PROJECT
FEASIBILITY STUDY IDEAS: STELLA SOFTWARE

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3 IDEAS: 1) 3 LEVEL SCREEN MAPPING
2)3) DISPLAYING NUMBERS, CHARACTERS
4) SCANNING A KEYBOARD.

1) 3 LEVEL SCREEN MAP IS NECESSARY FOR BOARD GAMES, DOMINOS, ~~BINGO~~ OTHELLO, CHECKERS, AND OTHERS.

STELLA MAPPER'S IDEA IS TO WRITE ALTERNATE IMAGES ON ALTERNATE FRAMES, SO THAT THE TOTAL SCREEN IS WRITTEN EVERY ~~2~~ 2 FRAMES.

3 LEVELS
— PF. WRITTEN ODD FRAMES
— BACKGROUND
— ~~BACKGROUND~~ PF. WRITTEN EVEN FRAMES

(1A) LARRY ~~KAPLAN~~ KAPLAN'S IDEA: TWO LEVEL SCREEN MAP.

1) TURN OFF OBJECTS.
2) WRITE RIGHT SIDE OF PLAYFIELD ON ONE FRAME, WITH COLUP0 = BACKGROUND COLOR, COLUP1 = SOME COLOR
3) 2ND FRAME, WRITE LEFT SIDE, COLUP1 = ~~0~~, COLUBK COLUP0 = SAME COLOR

CARE SHOULD BE TAKEN IN THE MIXING OF ~~COLOR~~ PF COLORS AND BACKGROUND COLOR

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GAME OR PROJECT
FEASIBILITY STUDY IDEAS:

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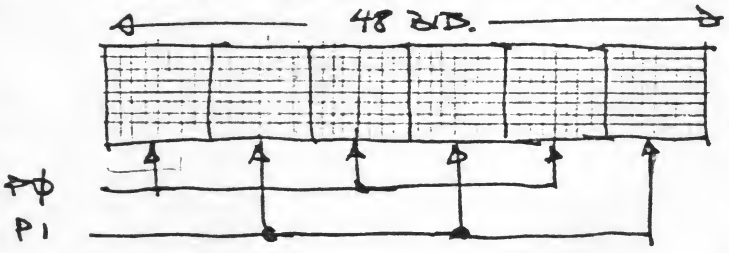
2)A DISPLAYING ~~NUMBERS~~.. CHARACTERS.

SIX CHARACTERS TOGETHER (AS IN A WORD.)



= 3/10 OF SCREEN.

P0, P1 SAME COLUM.

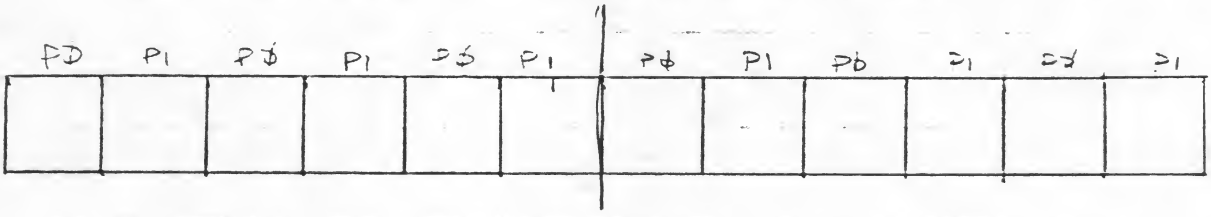
NUSIZ0 = 3
NUSIZ1 = 3

42 BYTES OF IMAGE. WRITTEN OUT REAL FAST.
6 BYTES / LINE

~~6 OF 7~~ (5x7) DOT MATRIX CHARACTERS.
6 to 8 (DEPENDING ON SPACE BETWEEN CHARACTERS)

IF YOU USE LARRY KAPLAN'S IDEA.

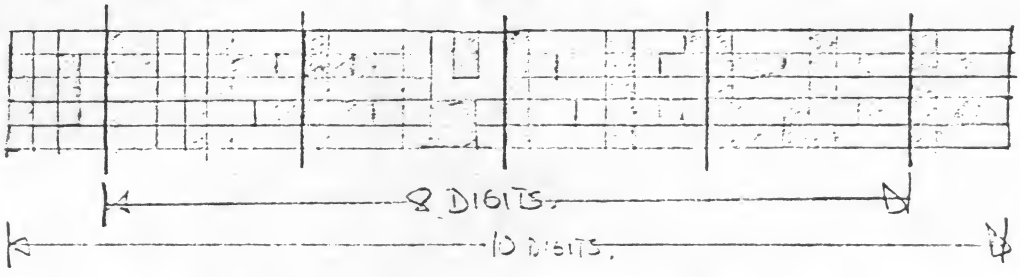
2B)



DO THE SAME THING, EXCEPT WRITE THE LEFT SIX BYTES ON ONE FRAME, AND THE RIGHT SIX BYTES THE NEXT FRAME.

3A) DISPLAY NUMBERS · AS 5x3 MATRICES. —
AS IN SCORE MODE NOW.

EITHER USING PLAYFIELD NOW:



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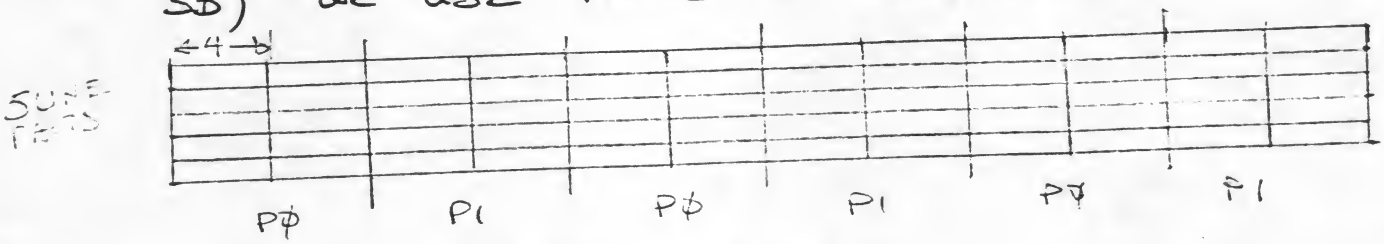
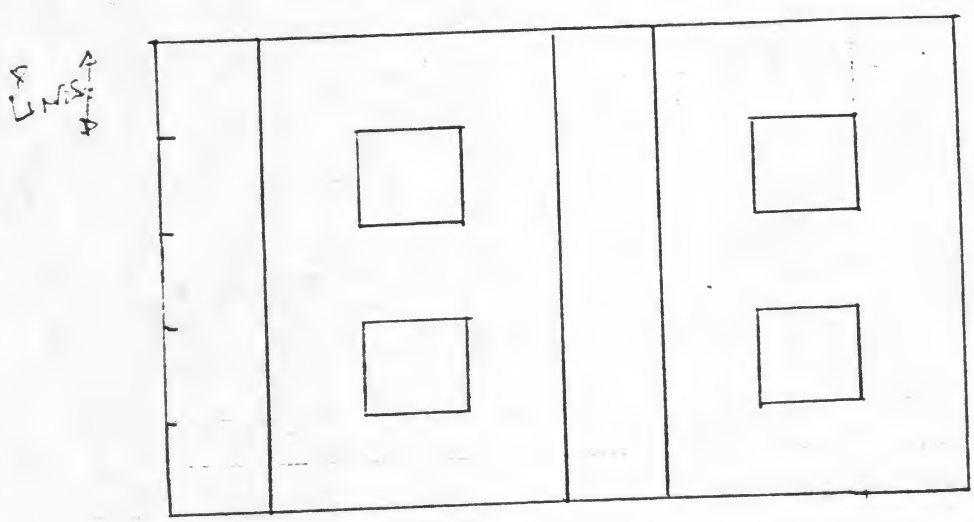
GAME OR PROJECT
FEASIBILITY IDEAS

3b) OR USE PLAYERS TO DISPLAY NUMBERS

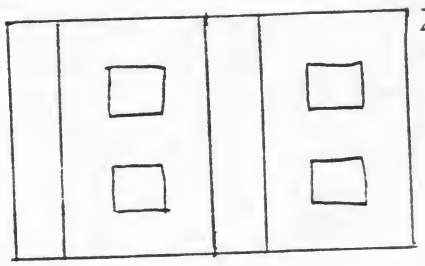


12 SMALL DIGITS.

OR 2 LARGER PAIRS



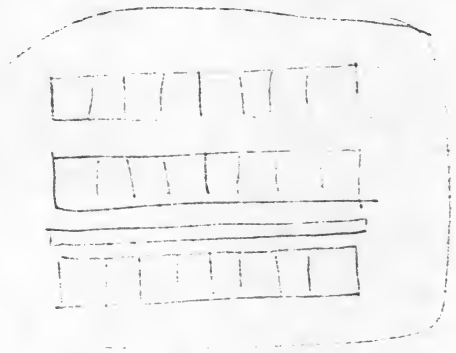
≠ 1 PLAYER.
×4



P 1 PLAYER
×2

ALL THIS IS GOOD FOR DISPLAYING SMALLER NUMBERS HERE AND THERE, OR EVEN

FOR IMPLEMENTING A CALCULATOR: !?



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GAME OR PROJECT
FEASIBILITY IDEAS.

4) KEYPAD.

THE CONTROLLERS HAVE A LOT OF WIRES.

1 8 BIT BIDIRECTIONAL PORT (NOT TRISTATE)

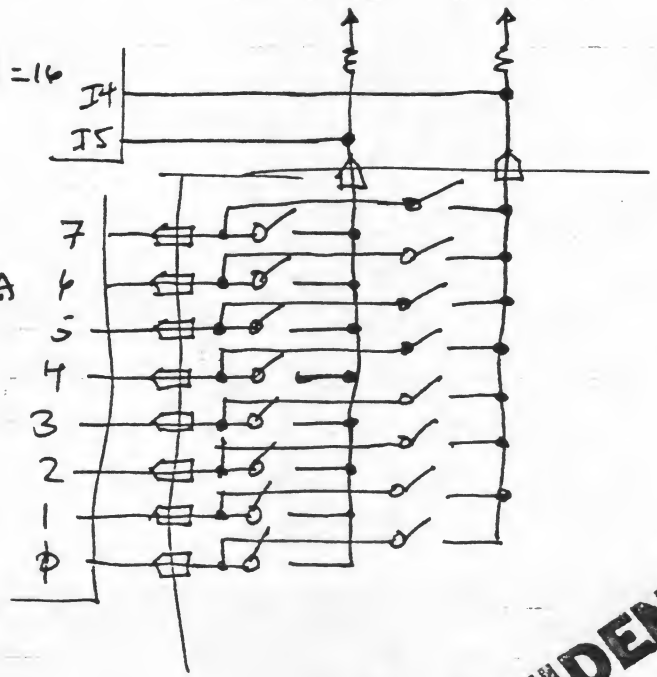
2 TIA INPUT PORTS - HIGH IMPEDANCE (PULLUPS INSIDE)

4 POT PORTS - (SLOW)

14 LINES

SEVERAL MATRICES:

a) 2×8=16



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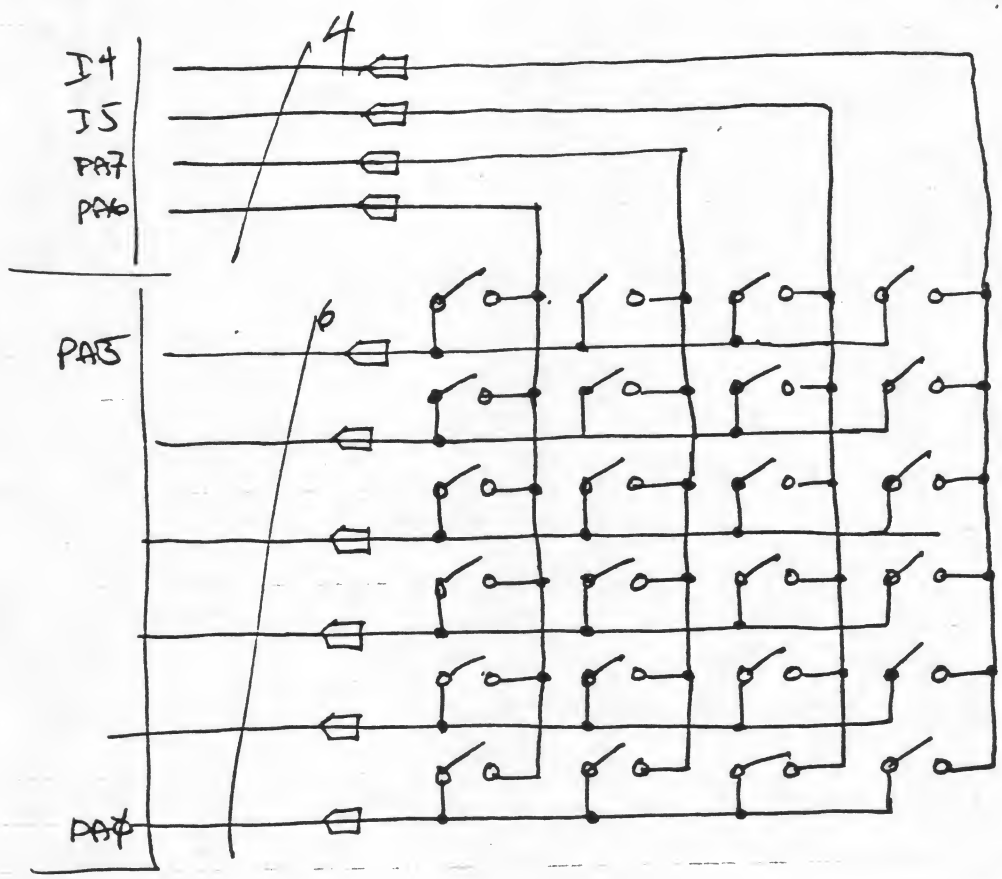
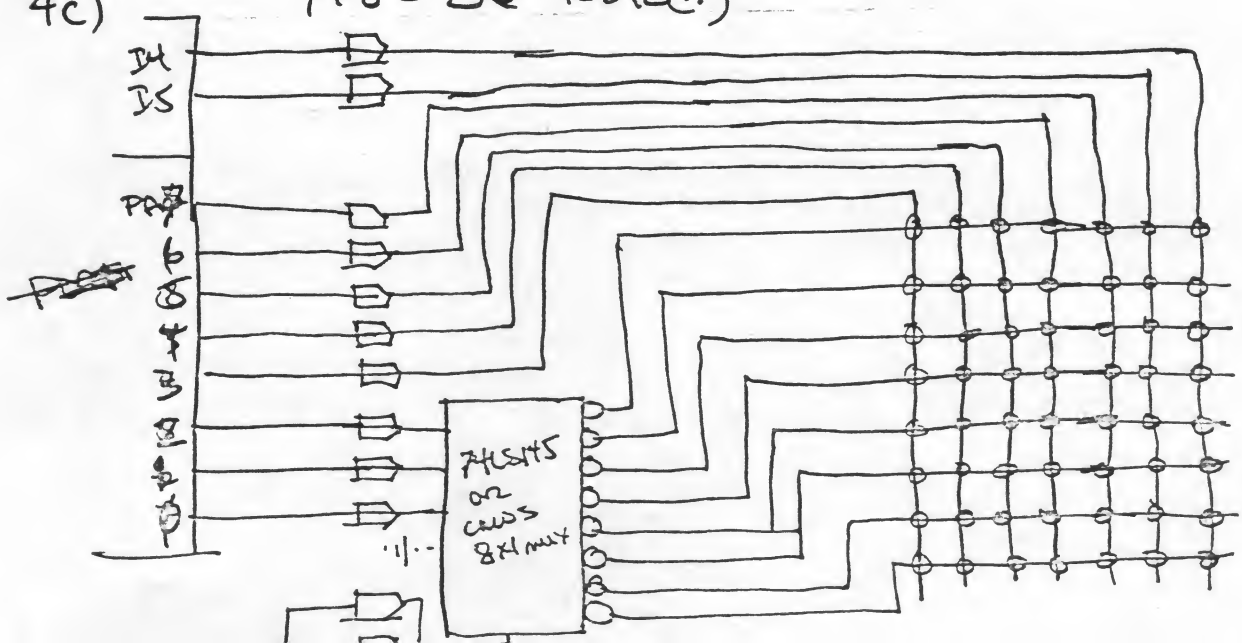
4b) 4×6 = 24



4c) 7×8 = 56 KEYS(!!)



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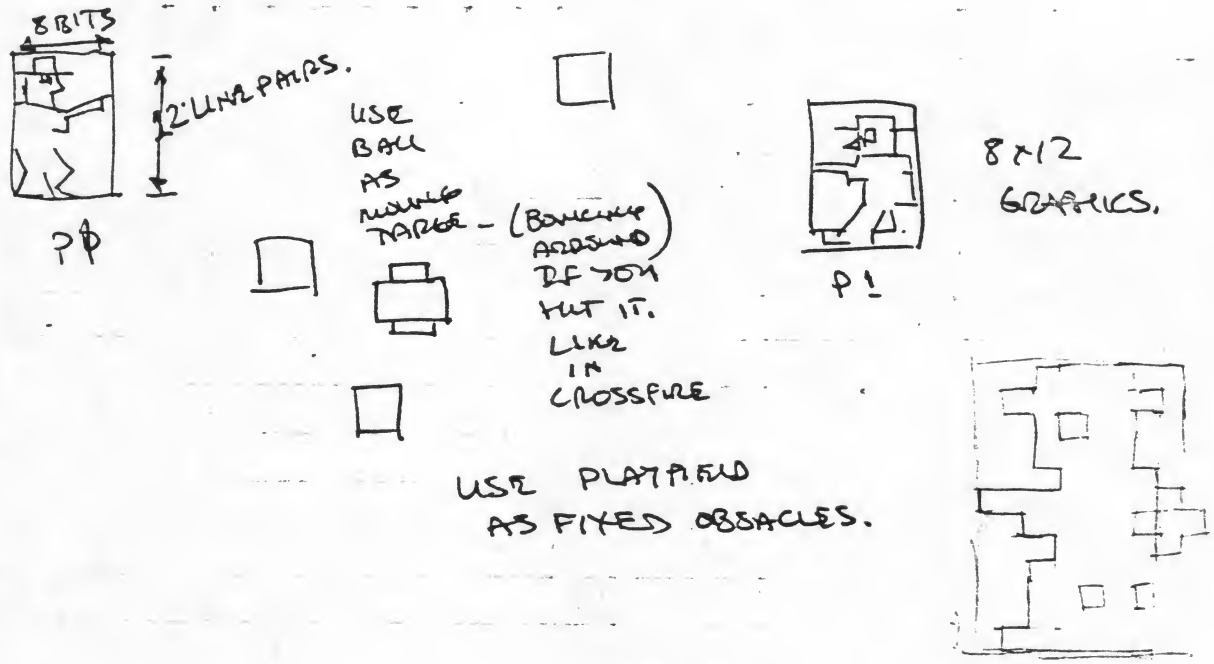
GAME OR PROJECT
NEW GAMES.

5) SOMEDAY, SOMEBODY OUGHT TO DO MIDWAY GUNFIGHT.


8 BITS
12 LINE PAIRS.
P0
USE BALL AS MOVING TARGET - (BOUNCING AROUND IF YOU HIT IT. LIKE IN CROSSFIRE
P1
8×12 GRAPHICS.
USE PLAYFIELD AS FIXED OBSTACLES.

6,7,8) STEEPLECHASE
SPACE RACE
DOMINOS
FLYBALL
ETC.

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BACK TO PADDLE GAMES:

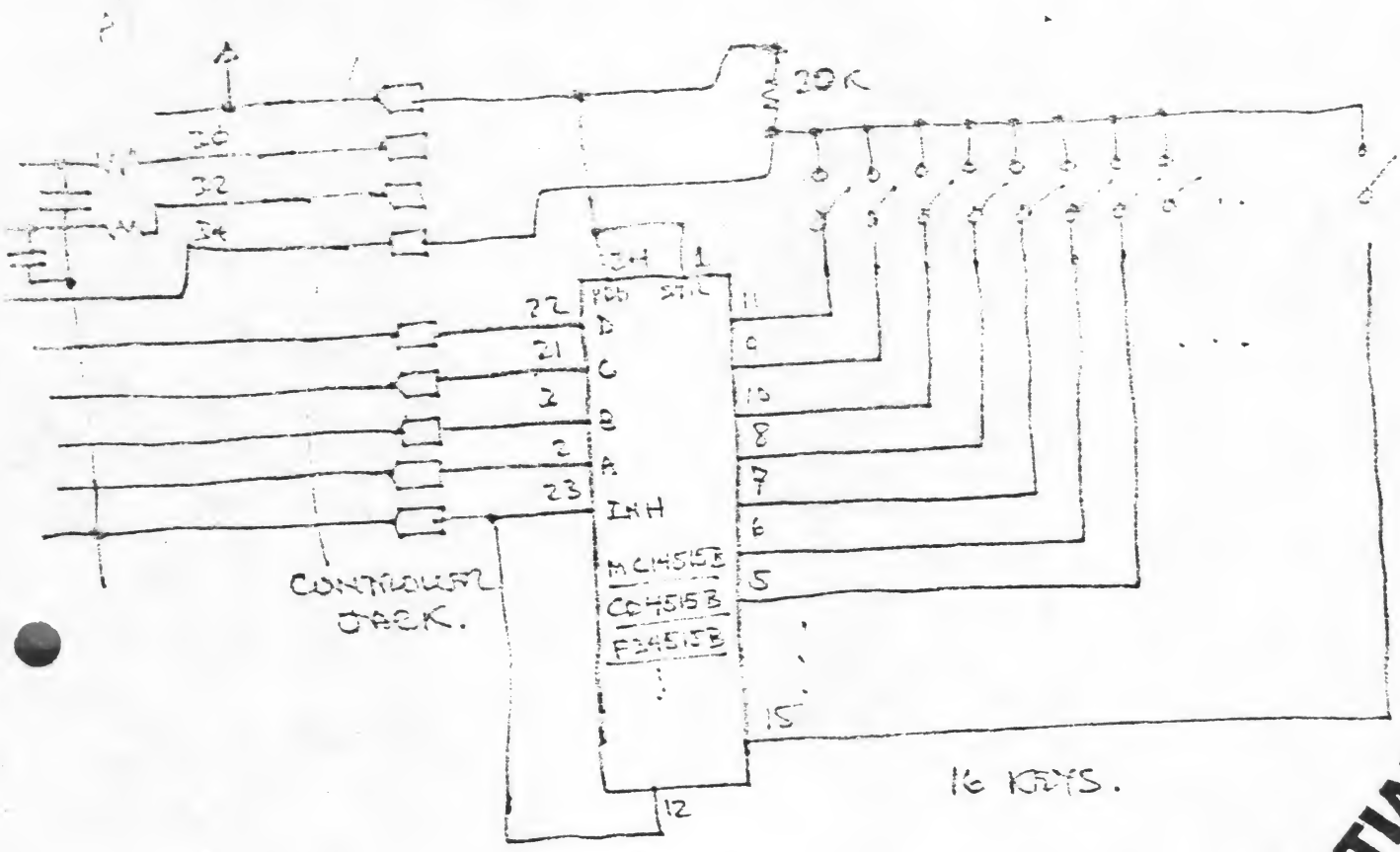
	BARRIERS	DIFFERENT PADDLE CONFIGURATIONS.
HOCKEY	X	
SOCCER	X	
PONG (TENNIS)	X	
HANDBALL	X	
BASKETBALL		
VOLLEYBALL		
QUADRAPONG.		

ADD GRAVITY TO HANDBALL?

WRITER DECUIR	DATE 12/5/77	WITNESS	DATE

GAME OR PROJECT

STELLA - 16 KEY KEYPAD.



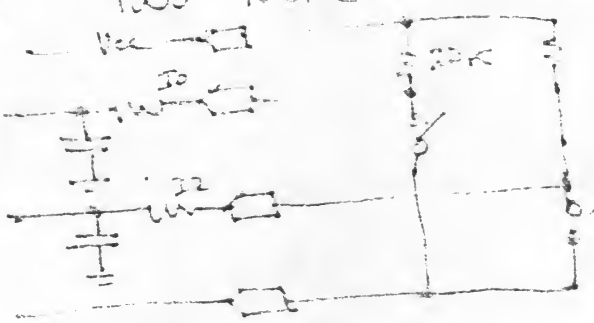
3)

$$\frac{5V \times .068\mu F}{.4\,mA} = \frac{5V \times .17\,mF}{A} = \frac{.85\,msec}{64\,\mu sec/LINE}$$

$64\,\mu sec/LINE$ $64\,\mu sec/LINE$

CONFIDENTIAL

TO GET TWO MORE KEYS.



BIG POT SCAN NEEDED INSIDE AT THE END OF FRAME BEFORE TURNING ON VBLANK

GAME OR PROJECT

CELLA - 16 KEY PAD.

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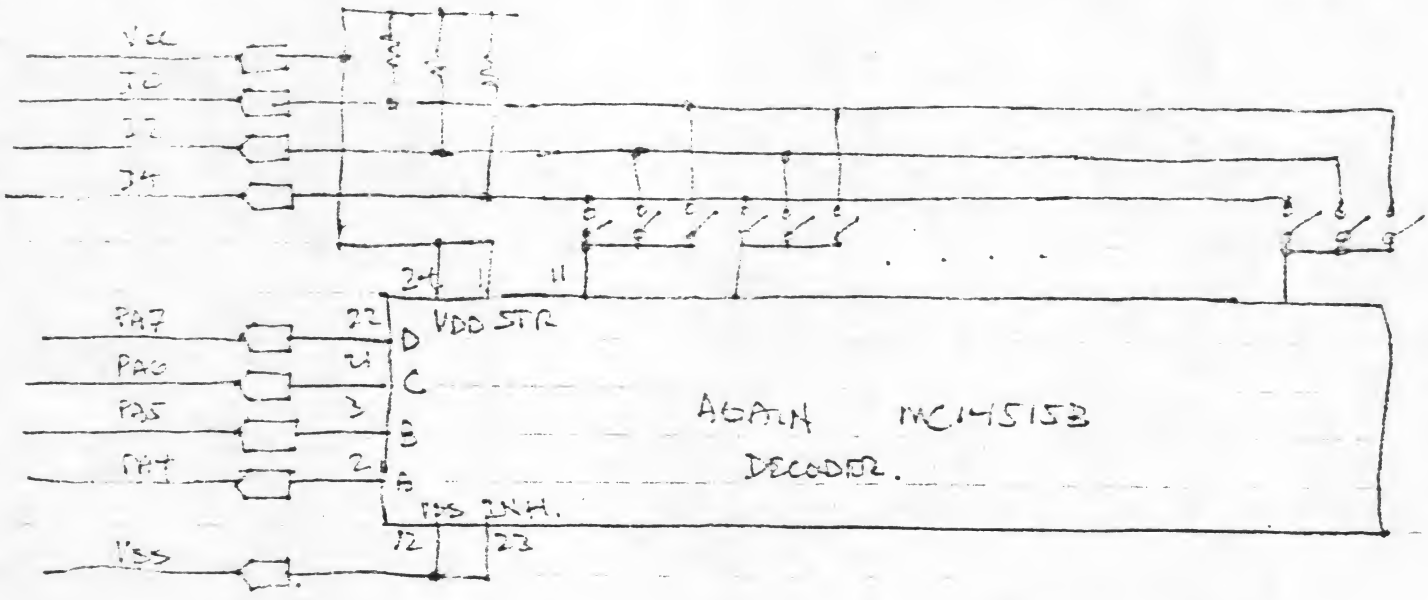
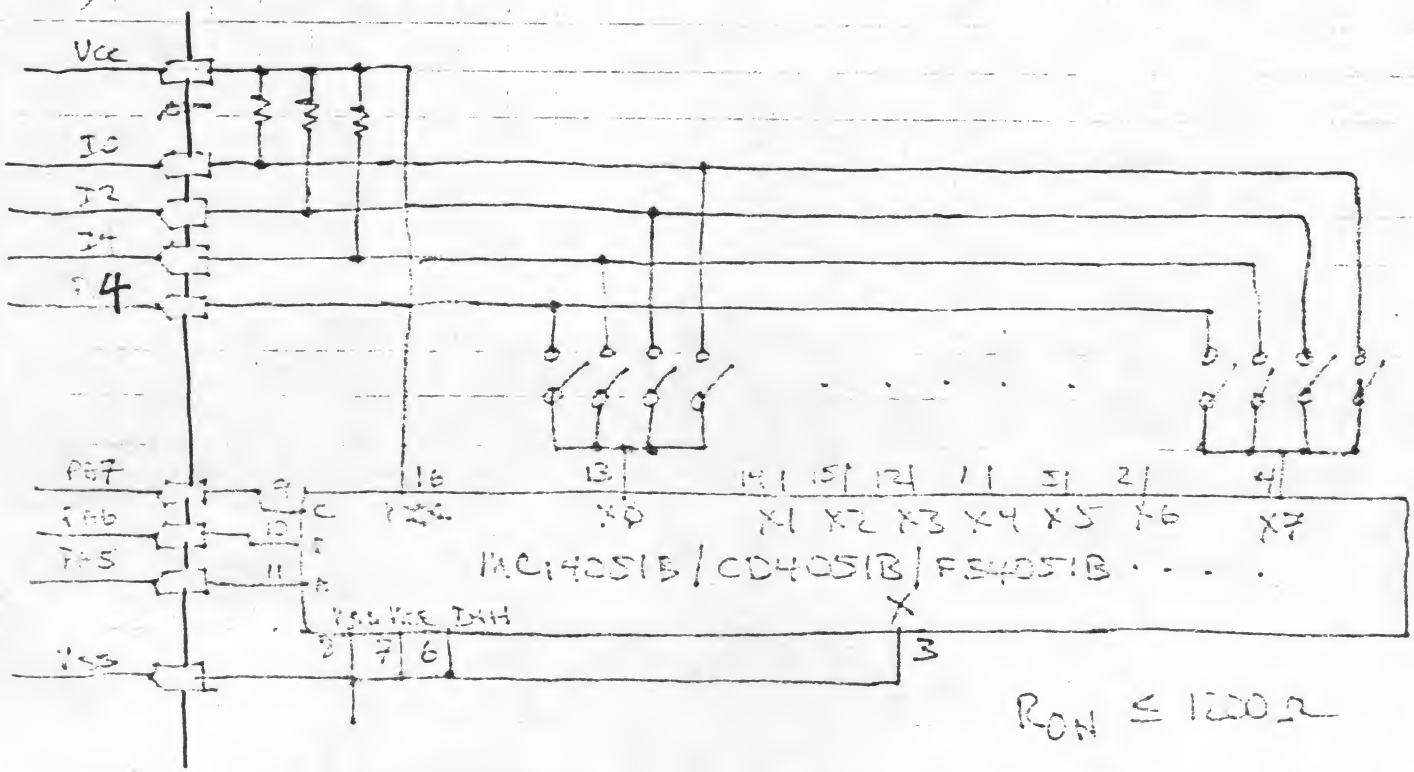
C)

OR EXPAND IT. 16×3 = 48 KEYS.



D) OR EXPAND IT DIFFERENTLY. 8×4 = 32 KEYS.



ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
STELLA -

CONFIDENTIAL

REMEMBER TO WRITE DOWN MY FTC PROBLEM SOLUTION:

IN ATTRACT MODE, FOR STELLA GAMES, GENERATE SLOW COUNTER. AND USE IT TO TOGGLE ALL COLOR AND LUMINANCE BITS TO EACH POINT, SO THAT ALL PLACES ON SCREEN GET ALL POSSIBLE LUMINANCE AND CHROMA LEVELS, RANDOMLY DISTRIBUTED, SO THAT THE TV DOESN'T GET BURNED IN.

CHARACTERIZE COLOR DELAY LINE

$V_{DEL} = V_{CC} = 5.02$ BURST DUTY CYCLE = 25/55 = 45%
GREEN (END) DUTY CYCLE = 20/55 = 36%

$V_{DEL} = 5.65$	GREEN DELAY	= 230 nsec
$= 3.02$	" "	= 280 nsec
$= 4.51$	" "	= 330 nsec

CHARACTERIZE SCHMITT TRIGGER INPUT PINS.

V_{EE} =	4.6V	5.03	5.4V
RISING THRESHOLD	1.90	2.02	2.05
FALLING THRESHOLD	1.42	1.45	1.45

GAME OR PROJECT

STELLA - 6532 PORTS. - CHARACTERIZATION.

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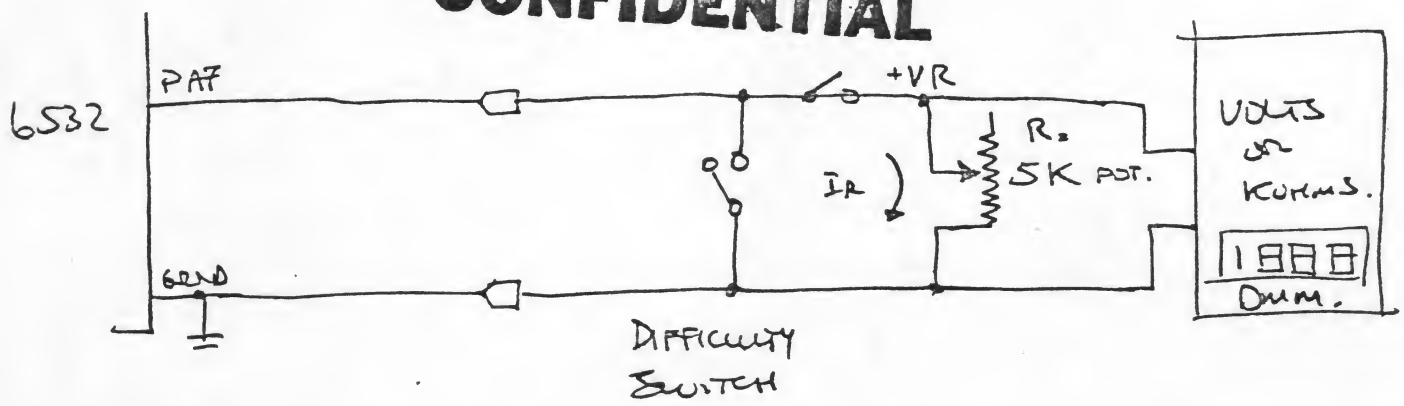
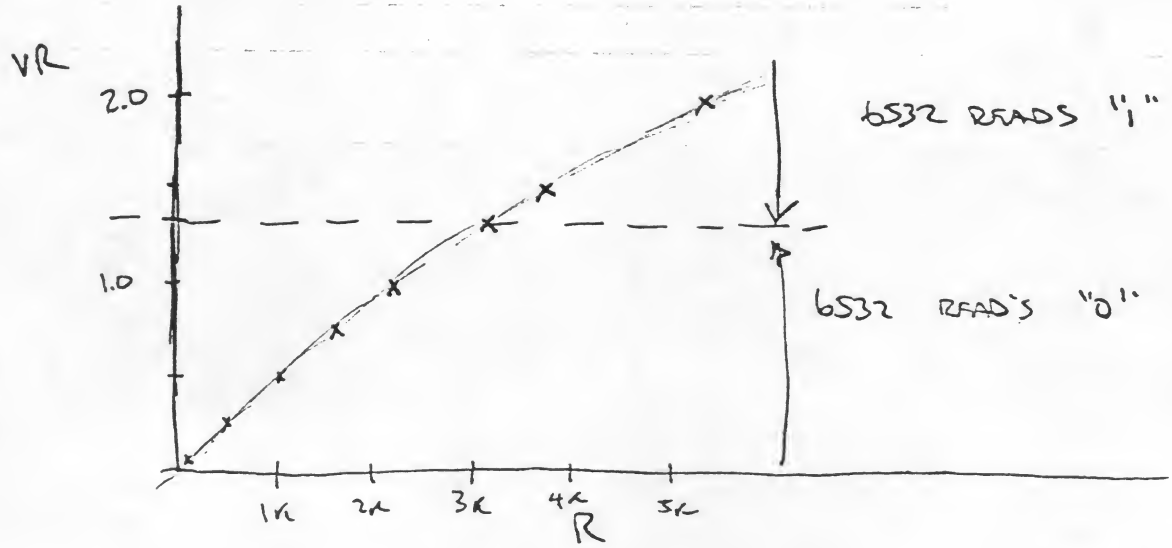
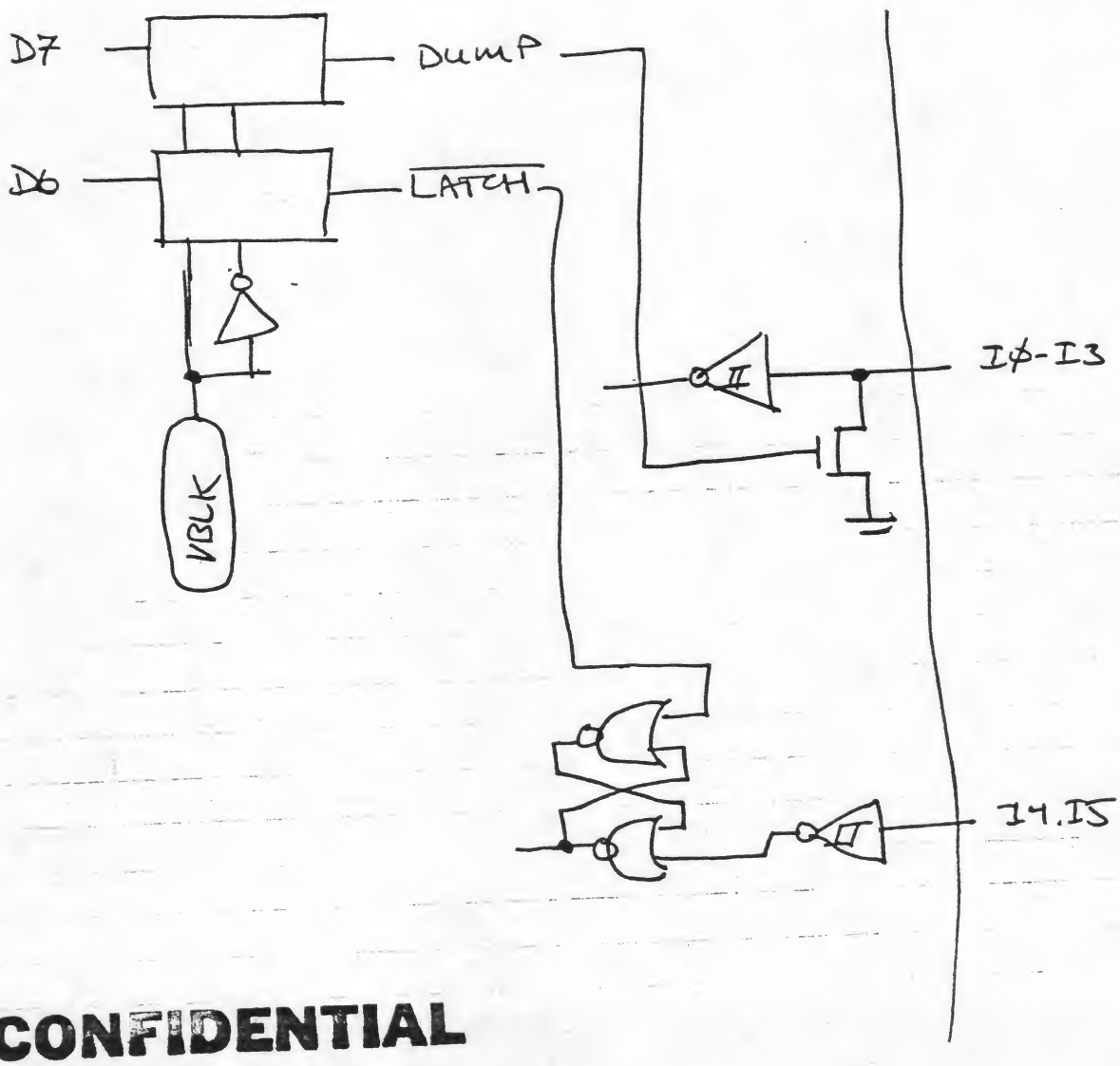


.53 mA	.006	.000
IR	VR	R
.476 mA	.10	.21K
.480	.25	.52K
.476	.50	1.05K
.465	.75	1.61K
.446	1.00	2.24K
.442	1.33	3.15K ← PB7 THRESHOLD.
.412	1.50	3.64K
.376 mA.	2.00	5.32K

VIRTUALLY NO HYSTERESIS OBSERVED IN 6532 PORT.



GAME OR PROJECT
STELLA - CHANGES TO CHIP.



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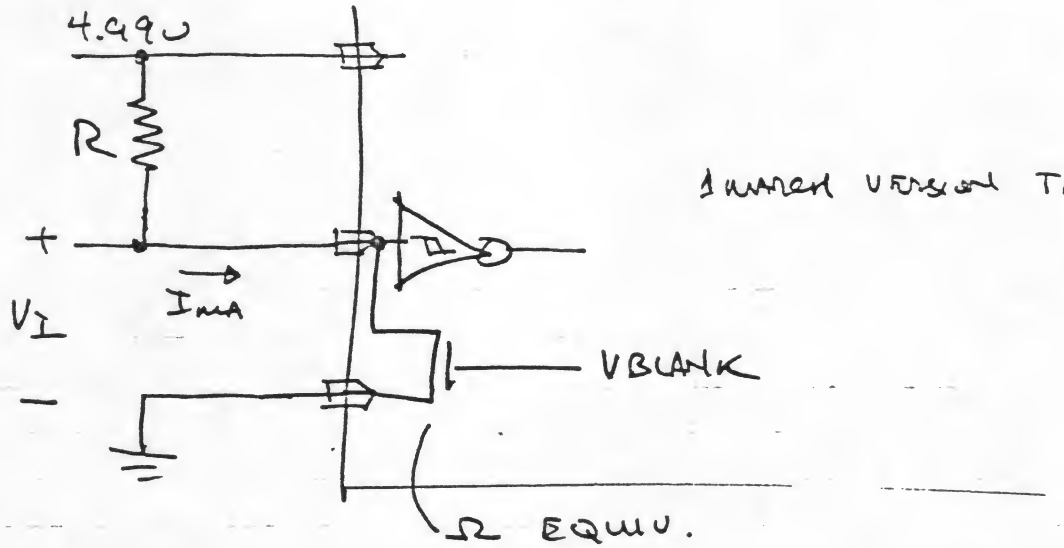
DATE

GAME OR PROJECT

STELLA - CHARATERIZE PORT PULLDOWN.



1 NMOS VERSION TIA

R(K)	V_I	I (mA)	Ω equiv.
4.71	.305	.995	306
3.87	.357	1.197	298
3.28	.407	1.397	291
2.67	.489	1.686	290
2.16	.588	2.038	289
1.78	.698	2.411	289
1.48	.824	2.815	292
1.18	1.010	3.373	299
.99	1.192	3.836	311

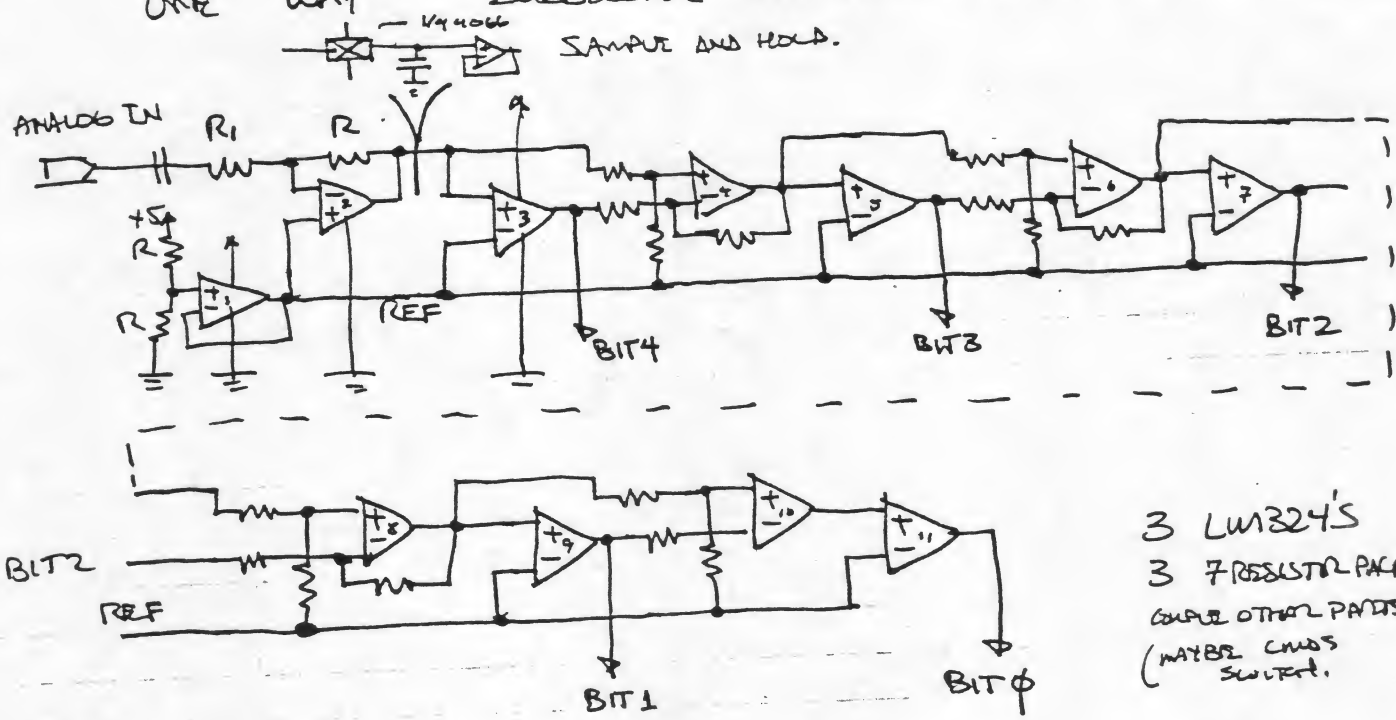
CONFIDENTIAL

WRITER JOSEPH DECUIR	DATE 8 MARCH 77	WITNESS	DATE

GAME OR PROJECT
STELLA -

PROBLEM. HOW TO DO FAST 5 BIT A-D W/ SINGLE SUPPLY AVAILIBLE. ON A CONTROLLER INPUT.

ONE WAY - SUCCESSIVE APPROXIMATION IN ANALOG:



3 LM324'S
3 7 RESISTOR PACKS
SOME OTHER PARTS (MAYBE CMOS SWITCH.

ALL AMPLIFIERS ARE, SAY NATIONAL LM324'S

THIS IS ANALOG SUCCESSIVE APPROXIMATION.

(ASYNCHRONOUS)

MIGHT NEED SAMPLING, W/ 12TH AMP AND CMOS SWITCH.

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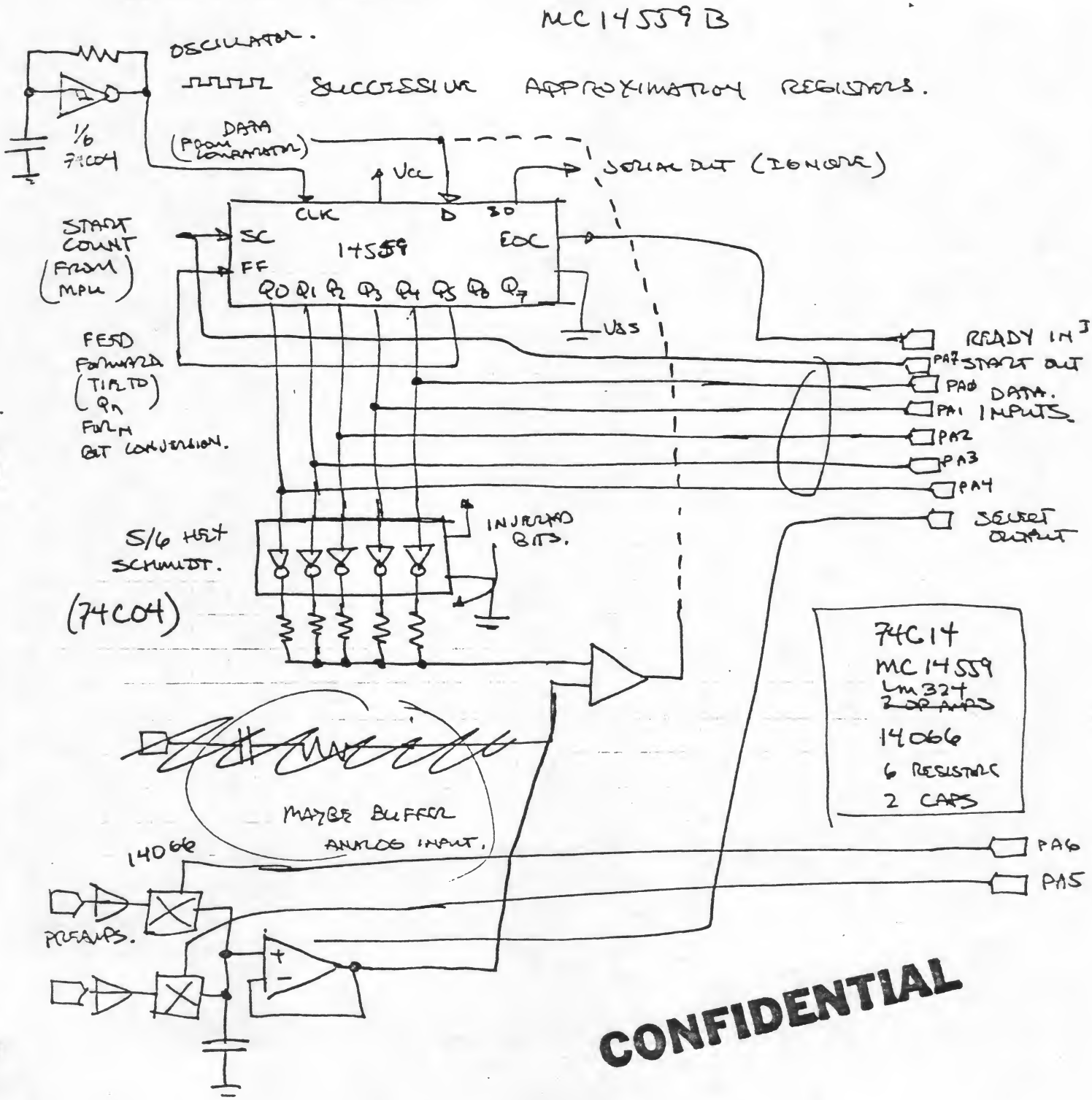
GAME OR PROJECT

STELLA -

CONSIDER MOTOROLA MC14549B
MC14559B



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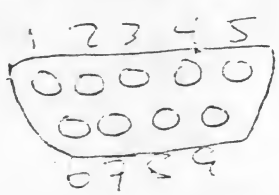
GAME OR PROJECT
STELLA



DE-9S'S.

14.AR277

1	FORWARD,	PA 4, 0
2	BACK	PA 5, 1
3	LEFT	PA 6, 2
4	RIGHT	PA 7, 3
5	POT 0, 2	
6	TRIGGER.	I4, I5
7	VCC	
8	GND	
9	POT 1, 3	

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DATE

GAME OR PROJECT

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WILL SEND UP BLOCK DIAGRAMS

CHARACTER SPACES

THEY WILL START ADVERTISING AGAIN

(6000 IN DESIGN AGAIN

(STARTING LOGIC DESIGN.)

SAMPLES FOR FEBRUARY

IT DOES NOT INVENT ANYTHING

CHIP FREEZE DATA LOSING

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

32

GAME OR PROJECT

CONFIDENTIAL

GAME OR PROJECT
NEW TECHNOLOGY · 800 & 5200

WILL WATCH FOR TEST, SIMULATION, BUG REPORT.

6600 FINAL SPEC
VIC
PARTS TO 'LOOK WITH' ROM.
07+32
16 BIT. 6509
VIC W/RESPECT TO ~~6502~~ 6004

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6600 -- $10 ART

FEBRUARY, MARCH PARTS.
PRODUCTION APRIL, MAY.

CPU - SAVE + INSTRUCTIONS TO RUN I/O PORTS.

DEVELOPMENT HEDUCUS INSTRUCTION!!!

REGISTER INDIRECT ADDRESSING MODE
AUTO INCREMENT W/ 16 BIT TIMER

TRYING TO OPTIMIZE THIS TO RUN VIC,

ROM/RAM ARRAY. (COMMON DECODE)
2K + 64

EXTERNAL MEMORY, 13 BIT PC

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
MUSIC TECHNOLOGY

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6800 - COULD BE A SPACE

WITH LOTS OF I/O
MAY BOTH ST + TIA
SPACE FOR DEDICATED CHIPS

(NOTE: PREVIOUS USES OF ANALOGS
FOR 6800 + TIA
6527 + 6810 + TIA.
FOR.

6509 " MORE OF A COMPUTER"

VIC REQUIRES ~200 SOME USEC ACCESS.

SYSTEM CPU.
6520 (?)
VIC. COMMODORE NOW 6540
RAMS + 6550/5 (+ SST)
NTSC, PAL OR SECAM.

VIC DOES
ON BOARD
VIDEO
SOUND

BIG AUDIO SYNTHESIZER

SAMPLES & AND SEQUENCER.

OR BUY ALREADY MADE

$45 FOR CHIP SET

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

DUAL SOUNDBOARD

CLOCK ON U.C.

DOT CLOCK AND CPU

DIFFERENT DUAL BOARD USAGE OF 14.318 MHz

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WRITER	DATE	WITNESS	DATE

CONFIDENTIAL

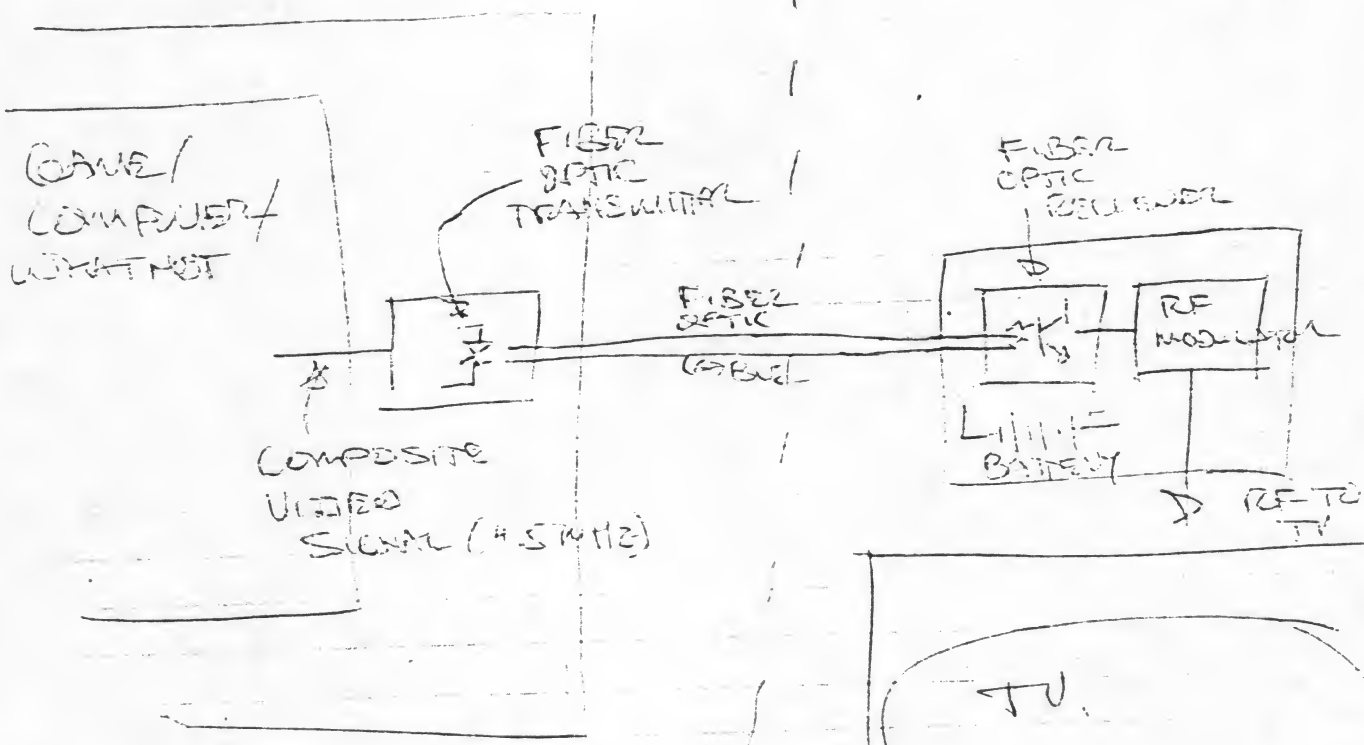
ATARI ENGINEERING LOG SHEET

36

GAME OR PROJECT
GENESIS

HOST ILLUSTRATION W/ CABLE TURN

METHOD FOR TRANSMITTING VIDEO TO DISPLAY TV VIA COMPUTER HOST PC.



ADVANTAGES: IF NO ELECTRICAL CONNECTION FROM GAME TO TV. PERHAPS GAME/CONTROL DOES NOT HAVE TO HAVE TYPE I APPROVAL.

	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

STELLA COST REDUCTION.

37

CONFIDENTIAL

14 JULY. MOS TECHNOLOGY,

RAY HIRT.

WILL MATHIS

JULES HERTSCH.

---

8 AU677 ~~COST ESTIMATE~~

CHIP SIZE ESTIMATE ON SEVERAL APPROACHES.

DELIVERY DATES FOR SAMPLE & PRODUCTION.

MONTH DELAY FROM MOS TECH TO SYNERTEK & ROCKWELL

1) (6507 + PARTS of 32)

2) (6507 + ~~R~~ I/O TIMER) + 6810.

3) (6507) + (REDUCED 32)

4) (6507) + (REDUCED 32 w/o RAM) + 6810.

VS 5) 6507 + 6532 AS IS.

6) #5) - W/O TEST FURTHER DOWN ON LEARNING CURVE.

PARTS of 32 we USE:

- PA, BIDIRECTION.
- PB. BITS INPUT.
- TIMER. ÷1, ÷8, ÷64

WRITER

DATE 14 JULY.

WITNESS

DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

6600

CAN BRING IN $\phi 2$ (1.2 MHZ)

IF YOU DON'T BRING OUT

ADDRESS MULTIPLEXED WITH DATA.

CAN BE BONDED (LAID OUT)

WITH. $\phi 2$.

CS

AS

.

Aϕ.

FOR STELLA.

CAN BE BONDED.

$\phi 2$	
CS	D7.
A6	.
.	.
.	.
.	.
Aϕ	Dϕ

CONFIDENTIAL

DATE

GAME OR PROJECT

6600

~~THOUGHT~~

TAKES 1 DAY TO RUN USERS TO LAY OUT PERIPHERY.

MAX SPEED.

MASK TURNAROUND IN 1 DAY - 1 WEEK

6-8 WEEKS FOR REASONABLE TURNAROUND.

TURNAROUND FOR DIFFERENT MASK.

IS THE SAME AS ANY PERIPHERY CHANGES.

SAMPLES IN FEBRUARY. - - -

EMULATE IT WITH 6522'S AND 6502, AND RAM AND ROM.

APPROXIMATE.

32×8	512×8
64×8	1K×8
128×8	2K×8

200 mil

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
6600

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EXPANSION COMPATIBLE W/ 8048

SUGGESTS 8041 TYPE DEVICE

VARIOUS DESIGNS TO INTERFACE W/ VIC. COMMA LATER.

MCENARNEY.
CHARPENTIER

CELLS ARE FIXED IN HORIZONTAL SIZE - BUT YOU CAN TURN OFF SOME OF THEM.

- PROBABLY GENERATES ADDRESSES OFF HORIZONTAL COUNTER.

CONFIGURABLE - 23-24 CHARACTERS ACROSS

LINE — x 240 lines — 517 WITH 8x8

14.3818 / 3.5 = 4.0809.

WITNESS	DATE

GAME OR PROJECT VIC.

CONFIDENTIAL

HORIZONTAL 258 CLOCKS

192 DOTS. EXAMPLE.

TURN OFF DISPLAY BY PUTTING IT OFF SCREEN.

NO INTERRUPTS FROM VIC -

TURN OFF SCREEN W/TIMER.

~~CPU RUNS @ 14/3.5/4.~~

16 BYTES OF CONTROL

0,1 HORIZONTAL AND VERTICAL POSITION OF TOP LEFT OF DISPLAY W/RESPECT TO VSYNC

HSYNC ÷81 FROM DOES INTERLACE.

2, 2,3, V.H. CHR SIZE COUNTER

COMES OUT W/ COMPOSITE SYNC, COMPOSITE LUM, COMPOSITE COLOR.

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
VIC

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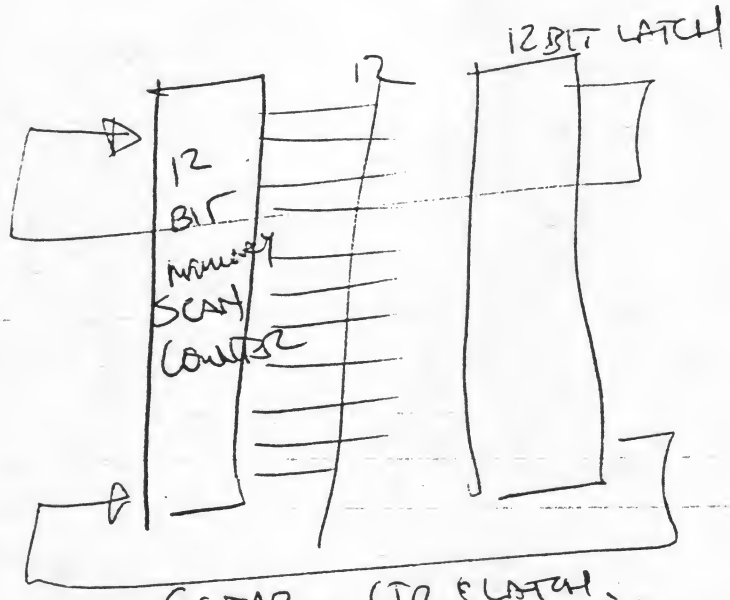
ADDRESS COMPUTATION.



CLEAR LTR LATCH.

COUNT UP.

JAM LOAD

COUNT UP

JAM LOAD

LINE OF CHARACTERS.

COUNT UP. AND RELOAD LATCH

JAM LOAD

COUNT UP.

(no H or V reflect)

WRITER	DATE 14 JULY	WITNESS	DATE

GAME OR PROJECT
VIC

2 POTS — 8 HORIZONTAL LINES PER CONVERSION 8 BITS.

US CHIP 6052B FOR EXPANSION.

~~LAST~~ REG A, B, C, D, E SOUND.

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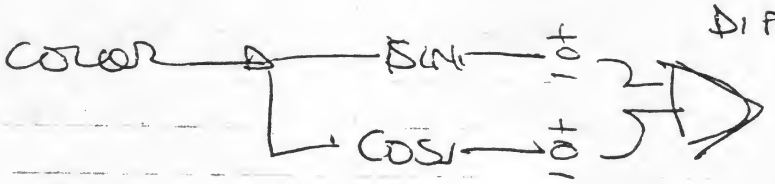
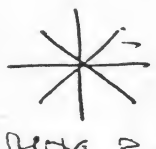
12 BIT WIDE MEMORY FOR COLOR.

QUADRATURE GENERATOR ON CHIP.



DIFF AMP ON CHIP.

8 COLORS



WHITE, BLACK & SIX COLORS

TWO CHIP CHROMA.

TWO CHIP LUM.

AUDIO. 3 SINE GENERATORS (7 BIT DIVIDERS) + 1 16 BIT POLYNOMIC CTR.

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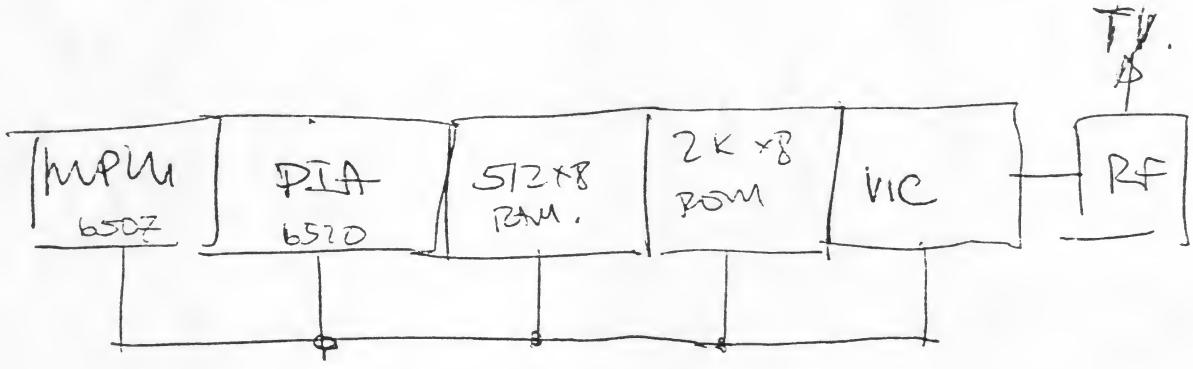
ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ADDA



30 CHAR / 14 LINES

PERHAPS CHANGE VIC
TO RUN AT SLOWER CLOCK -
TURN OFF PROCESSOR
TO ALLOW DOUBLE
FREQUENCY OF CHARACTERS.

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WRITER	DATE	WITNESS	DATE

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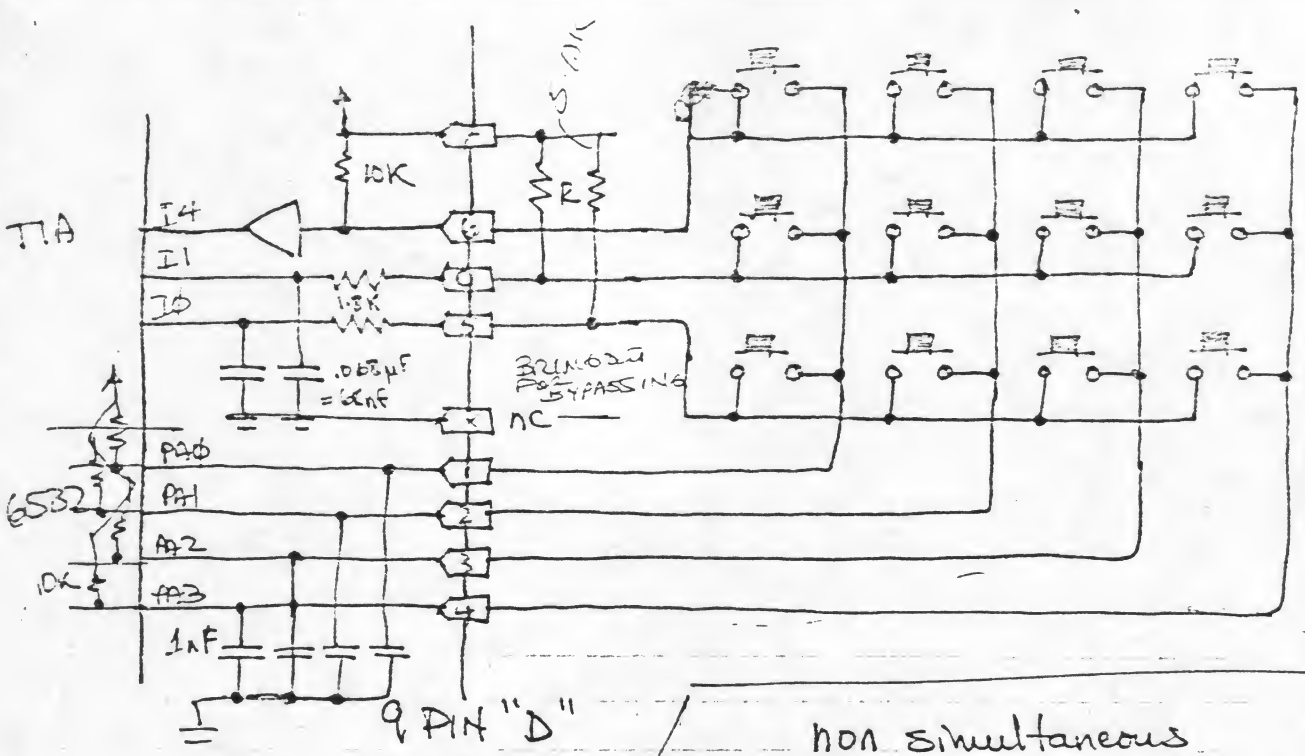
GAME OR PROJECT
KAY - 12 KEY KEYBOARD



non simultaneous - ie. single - keys can be detected by writing a single "0" AND 3 "1"s ON PORT A. AND, AFTER SUFFICIENT CHARGING TIME, READING I0, I1, AND I4 FOR "0"s

IF TWO KEYS ARE DETECTED SIMULTANEOUSLY, IGNORE ALL OF THEM. DETECT A KEY WHEN A SINGLE KEY GOES ↓

6532 PORTS CAN SOURCE .53 ma into 0 VOLTS - ⇒ (see p25 this notebook) . - look like 10K resistor pullups.

if all switches are closed one PA port has to sink 6 other pullups. 6 × 5V/10K = 3ma. ⇒ IT will CHOKE.

if pullup R on I0 AND I1 = 10K - it takes

00	⇒ 11101110	EE
01	: 11011101	DD
10	: 10111011	BB
11	01110111	77

WRITER	DATE	WITNESS	DATE
JOE DECUIR	July 77		

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GAME OR PROJECT
KAY.

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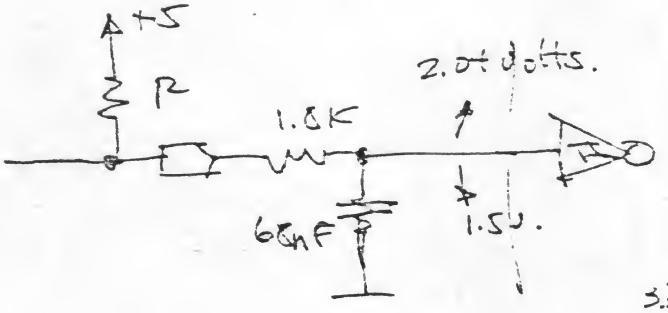
CHOICE of PULL-UP RESISTOR

pulling up.



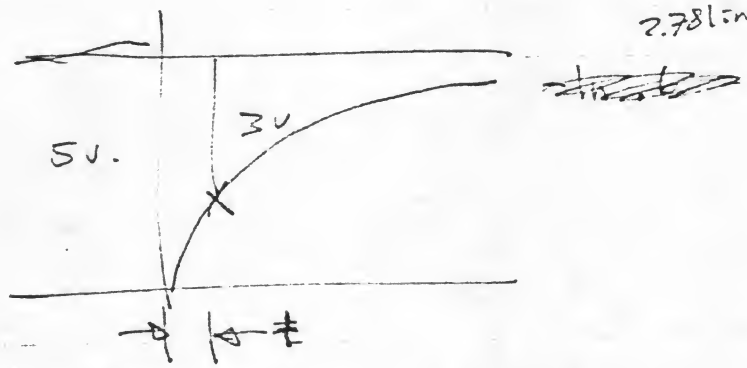
0.4 time constants

$-RC \ln .6 = t = 410 \mu sec.$ if $R = 10K$.

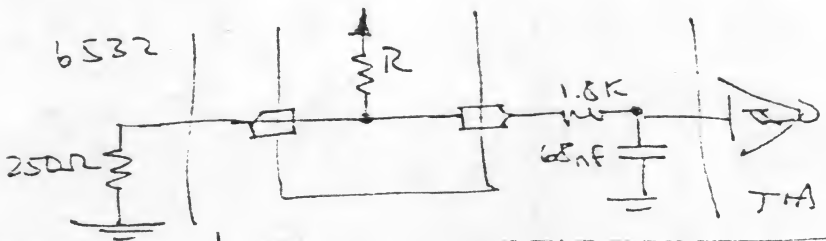
3.7 time constants

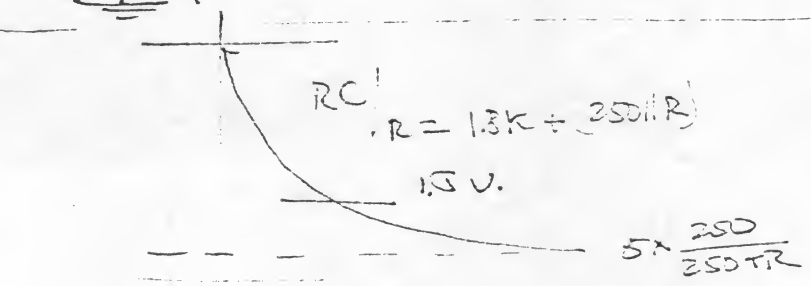
2.78 time constants. $= 236 \mu sec$ @ 5K

$= 177$ μsec @ 3.3K



pulling down.





WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
K24

250 || 10K = 244 Ω

250 || 5K = 238 Ω

250 || 3.3K. = 234 Ω

244 + 1.8K =

~~2.044~~ 2.044

$R = a\ 2K \times 68nF = 136\mu sec. = t$

× ×
× ×

if R = 5K $\frac{250}{5.25K} \times 5V. = \frac{5.00}{.238}$ volts.

⇒ 181 μsec. = 1.328 × 136 μsec.

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WRITER	DATE	WITNESS

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
PAL STELLA

EXPERIMENT

1) DISCONNECT AUDIO IN MODULATOR NETWORK FOR 6-D KIM SYSTEM (MOUNTED ON BOARD)

2) TWEAK MODULATOR FOR 67.25 MHz.

3) CONNECT RF OUT TO GRUNDIG TV-SET TO CHANNEL 3.

4) ADD LINES TO VERTICAL BLANK AREA IN COMBAT GAME CODE.

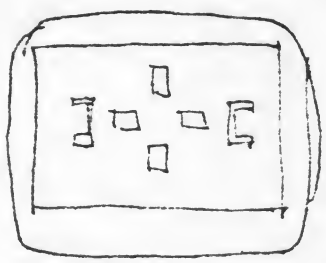
314 LINES OF FRAME.

DERIVATION.

$$\frac{\frac{3579575\ Hz}{228}}{50} = 313.99517 \text{ LINES/FRAME}$$

LOOKS OK !!

TANK ASPECT RATIO OK.



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WRITER JSCOLA	DATE 19 JULY 77	WITNESS	DATE

GAME OR PROJECT

PAL STELLA

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$4.43361875\ Hz. \times \frac{4}{5} = 3.546894.9\ Hz$

$\div 228 = \frac{15,556.556\ KHz.}{15.6113}$ @ $\frac{1}{1.0035}$

625 IS SPEC.

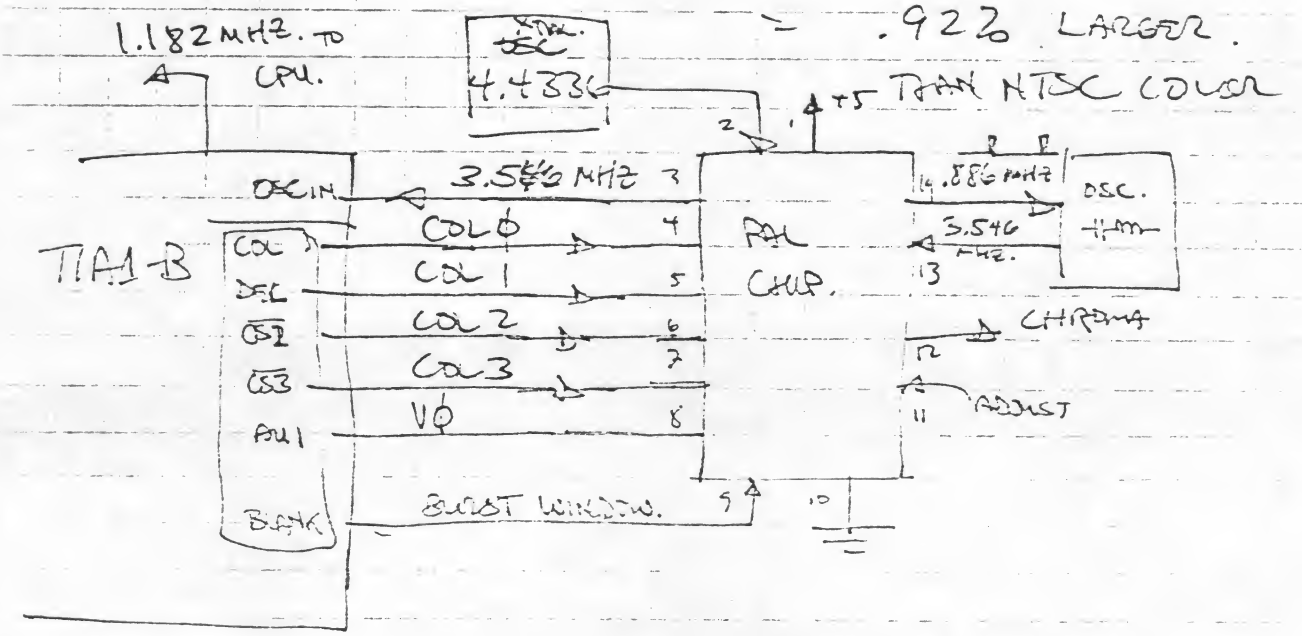
.35% ERROR. M H

$\frac{15556.556\ Hz}{50\ Hz} = 311.13113$ LINES/FRAME.

602 VS 625

$\frac{3.5795454\ MHz}{3.5468949\ MHz} = 1.009205$

$= .922$ LARGER.



JAY MINER

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
MOTOROLA 6809

FRANK MAHONEY SYSTEM

SKIP STRUNK SYSTEM DESIGN

JOEL BOREY SYSTEM DESIGN

BOB NOBIS PLANNING.

OVERVIEW: | 3 temp ranges
3 speed ranges
Fair | mil spec
HITACHI | Same Facet | new peripherals
new memory support
new memory
new interface
1,2 chip minimum systems 6801; 6802+6846
high performance upgrade of 6800

2ND QTR 78

MUST up for renewal in Oct '77

Source ~~comp~~ compatible - but not object compatible

95% DESIRED - commit spec at end QTR 77

INTRODUCE 3RD QTR 78

CONFIDENTIAL

WRITER JOEL BOREY	DATE JULY 77	WITNESS	DATE

GAME OR PROJECT
MOTOROLA 6809

5V CHIP CLOCK. 5V, BUS COMPATIBLE

8 BIT WORD SIZE 16 BIT ADDRESS

2MHZ MINIMUM CLOCK TARGET 200 mil

NO illegal opcode

MEMORY RDY.
INSTRUCTION SYNC
BUS REQUEST, BUS GRANT } PERHAPS HANG THE CLOCKS.
FAST IRQ (JUST PC AND STATUS)
PLEASE ADD AT LEAST ONE ACCUMULA

TWO IRQ PINS.

IRQ ACKNOWLEDGE. — VECTOR SELECT
IRQ MAY BE VECTORED BY DEVICE
"2MHZ" requires 225 nsec accesses.
— increase size of address drives.
to save cost of memory.

HALT →		← RES
SYNC ←		← XTAL
IRQ →		← EXTAL
FIRQ →		← READY
NMI →		→ Φ2
ACK ←		→ GRANT
VSS }		← REQ
VDD }		→ R/W

AΦ - A15
DΦ - D7

Keep data, address, Φ2, R/W for analyses.

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ASTEROIDS DELUXE

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TWO ACCUMULATORS.
TWO INDEX REGISTER
TWO STACK POINTERS - 1 AS IN
FAIRCHILD 3850 ARCHITECTURE
DIRECT PAGE POINTER

16 BIT WIDE

NOT doing low byte - high byte
chip designer wanted to do it
NOT source compatible

---

upward source compatible.
80 instruction — consistent mnemonics.
1 & 2 byte opcodes
348 OP CODES
8x8 multiply — UNSIGNED A*B → A,B / mostly for index calculations
16 bit operations
bit manipulation in memory
powerful stack instructions
register transfer & exchanges.

ADDRESSING MODES

11 ADDRESSING MODES

DIRECT VIA PAGE POINTER
INDIRECT ADDRESSING ADDED TO INDEXED MODES.
UP TO 16 BIT SIGNED INDEXED OFFSET.
AUTO INCREMENT, DECREMENT
ACCUMULATOR INDEXING. A+X →

2's of offsets -128 to +127

A,B + 2 BYTES IN MEMORY.

PC CONTENTS OR DP, DEX →
create add immediate to index registers.

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

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- POSITION INDEPENDENT CODE (16 BIT BRANCH AVAILABLE)
- NON SELF-MODIFYING CODE
- STRUCTURED, HIGHLY SUBROUTINED CODE
- MULTI-TASKING AND MULTIPROCESSING
- STACK ORIENTED COMPILER INSTRUCTIONS
- OPERATING SYSTEM CALLS. - 32 BASIC INSTRUCTIONS.

3 DIFFERENT REGISTERS } 2 8 BIT CALLS, 1 16 BIT CALL.

RES, IRQ, FIRQ, NMI, SWI.
OSC 1, OSC 2, OSC 3.

8 BIT

A	B
DIRECT PAGE PTR	COND. CODE REG.
IX	
IY	
US	
SP	
PC	

DECREMENT & BRANCH NOT EQUAL INSTRUCTION.

LOAD MEMORY IMMEDIATE

ADDRESSING MODE:
DATA.

IMPLIED
IMMEDIATE
DIRECT
EXTENDED (ABS)
INDEXED : 5 BIT CONSTANT OFFSET
8 BIT CONSTANT OFFSET
INDIRECT OFFSET
" AND ACCUMULATOR
" AND AUTO INCREMENT

ALSO LOAD EFFECTIVE

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

6809 OPTIMAL INSTRUCTIONS

CONFIDENTIAL

- POSITION INDEPENDENT CODE (16 BIT BRANCH IN RANGE)
- NON SELF-MODIFYING CODE
- STRUCTURED, HIGHLY SUBROUTINED CODE
- MULTI-TASKING AND MULTI-PROCESSING
- STACK ORIENTED COMPILER INSTRUCTIONS
- OPERATING SYSTEM CALLS. - STACK INSTRUCTIONS.
  3 DIFFERENT LEVELS } 2 8 BIT CALLS.
  1 16 BIT CALL.

RES, IRQ, FIRQ, NMI, SWI.
OSC1, OSC2, OSC3.

8 BIT

DIRECT PAGE PTR	COND. CODE REG.
A	B

IX
IY
US
SP
PC

DECREMENT & BRANCH NOT EQUAL INSTRUCTION.

LOAD MEMORY IMMEDIATE

ADDRESSING MODE: DATA.

- IMPLIED
- IMMEDIATE
- DIRECT
- EXTENDED (ABS)
- INDEXED : 5 BIT CONSTANT OFFSET
  - 8 BIT CONSTANT OFFSET
  - 16 BIT CONSTANT OFFSET
  - " A REG. ACCUMULATOR OFFSET
  - " B REG. ACCUMULATOR OFFSET

ALSO LOAD EFFECTIVE

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

[illegible]

THERE EXISTS A
DOUBLE LENGTH [illegible]
AND BRANCH
AND 8 BIT LONGITY

16 BIT INSTRUCTIONS.

DOUBLE ADD
" LOAD
STORE
COMPARE
SUBTRACT
DECREMENT, ~~INCREMENT~~ MEMORY
AND BRANCH NOT EQUAL
SIGN EXTEND. SEX [illegible]

BIT MANIPULATION
- BIT SET - OR W/ MEMORY
- BIT CLEAR - ~~AND~~ [illegible]
- BIT TEST
- TEST & SET
- BIT TOGGLE - XOR W/ MEMORY.

RELATIVE INSTR.
- LOAD RELATIVE REGISTER
- LOAD BRANCH TO SUBROUTINE
- LOAD BRANCH ?

?!!

CONFIDENTIAL

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

METEOROIDS

THERE EXISTS A
DOUBLE LENGTH MEMORY INCREMENT
AND BRANCH
AND 2 BIT LENGTHS

---

16 BIT INSTRUCTIONS.

DOUBLE ADD
" LOAD
STORE
COMPARE
SUBTRACT
DECREMENT, ~~INCREMENT~~ MEMORY
AND BRANCH NOT EQUAL
SIGN EXTEND. SEX MNEMONIC

BIT MANIPULATION
- BIT SET - OR W/MEMORY
- BIT CLEAR - ~~AND~~
- BIT TEST
- TEST & SET
- BIT TOGGLE - XOR W/MEMORY.

RELATIVE INSTR.
- LOAD RELOCATION REGISTER
- LONG BRANCH TO SUBROUTINES
- LONG BRANCH ?

?? !!

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WRITER	DATE	WITNESS	DATE

GAME OR PROJECT

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- PUSH ALL REGISTERS
- PUSH ONLY SOME REGISTERS
- PULL FROM U/S
- PULL FROM U/S
- INDEXING FROM U/S NOT IN U/S
- FAST EFFECTIVE ADDRESS

SUBROUTINES & INTERRUPTS

- RETURN USING U/S
- RETURN FROM FAST IRQ
- STOP & CALL IT SYNC
- OPERATING SYSTEM CALLS (?)
- SOFTWARE EXECUTION OF IRQ, FIRQ, NMI

} PASSING PARAMETERS IN CODE

(STILL HAS WAIT FOR INTERRUPT)

ISR DATA

→ DETAIL.

SOFTWARE RESET

SHOULD RESET WHOLE SYSTEM.

REGISTER

- TRANSFER REGISTER TO REGISTER
- EXCHANGE 2 REGISTERS
- ADD TO X, Y, U, or S immediate
- AND A to X, Y, U or S
- LOAD, STORE, ST, DSR, AND COMPARE WORD
- LOAD STORE A, B, X, Y, U, S, CCR, D, DP
- COMPARE X, Y, U, S, and D

MISCELLANEOUS

- SWI → IG A x B → B, A
- DECR & BRANCH NOT ZERO
- DECIMAL ADD A or B
- DECIMAL SUBTRACT A or B
- [illegible] TO MEMORY.

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

[illegible]

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BUILDING BUILDING

A 68K BASED EMULATOR
TO PLUG INTO EXERCISER.

2 Z80's + MICROCODE

QUESTIONS ABOUT HIGHER LEVEL
LANGUAGE

TOM ADDIE
TEXAS INSTRUMENTS
DM 1048 FIBER OPTIC XMITTER/RCVR 10ft LINK
$175 BOOK DELIVERY 4/20
776 PALOMAR
SUNNYVALE, CA 94086
732-1840

MIDI976:

100K	6.55
250K	4.88
500K	3.90
2M	3.75

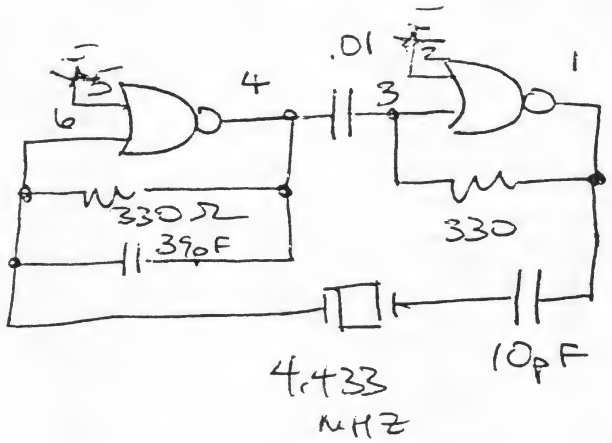
WRITER [illegible]	DATE [illegible]	WITNESS	DATE

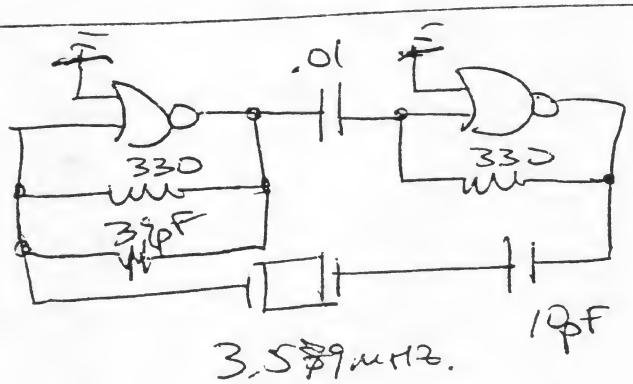
GAME OR PROJECT
PAL STELLA

TEST CIRCUIT FOR JAY'S

LOCKED OSCILLATORS IDEA:

OSCILLATORS:





3.579 MHz.

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WRITER	DECUR	DATE 2-5-07	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
Texas Instruments 9900

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they will produce 2 new members of 9900 series, which will specific to particular market segments

get our opinions on things that are useful for us.

they are 2nd sourced w/ AMI

review of 9900 ARCHITECTURE.

LOOK INTO CRU DETAILS.

I/O IS CRU of memory mapped.

ADDRESSING MODES
WORKSPACE REGISTOR
DIRECT REGISTOR
INDIRECT WITH AUTO INCREMENT
INDEX immediate register
SYMBOLIC (DIRECT)
IMMEDIATE
PC RELATIVE (JUMP)

WRITER	DATE	WITNESS	DATE
[illegible]	1977		

GAME OR PROJECT
TMS 9900

ALU

PROGRAM COUNTER

MOVES

LOGICAL

SHIFTS 1 bit shifts

I/O (CRU control)

RETURN

---

3 MHz clock 500 ns memory.

BRANCH	2.67	
ADD	4.67	R-R
MPY.	17 μsec.	16×16
DIV.	41 μsec.	16×16 !!
MOV	7.33	reg to direct ex

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60

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
TI 9940

SBP 9900 I²L 9900

TMS 9930 MULTIPLEX DATA BUS.
14 ADDRESS LINES.
ON CHIP CLOCK !!

TMS9940 SAMPLES IST QTR '78

128 BYTES RAM
2K ROM OR CHIP OR EPROM
4 INTERRUPTS IN
16 BITS OF CRU.
32 GENERAL I/O LINES
+5V.
256 BITS EXPANSION.
POWER DOWN MODE
SMART OPERATION
clock oscillator on chip
14 BIT TIMER
PIPELINED 8 BIT MACHINE INTERNALLY.

See 9940 writeup.

8 XOP's — SOFTWARE INTERRUPTS.

MULTIPROCESSOR INTERFACES
- serial port from, to another device bit rate [250-300 psec/word] 2.5 mHz.

separate power for ram, flags, registers and for everything else

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WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
TI 99/40

est (290 mil)^2 est $10 price "design goal"

good controller
poor memory expansion.

Kevin McDonagh. Dmos, NMOS FET (ISS solid state)

new processors

99XX 64 PIN PLASTIC PACKAGE

⇒ MULTIPROCESSING
EXTENDED ADDRESS SPACE (separate memory management)

MICROPROGRAMMED ARCHITECTURE

⇒ FLEXIBLE INSTRUCTION SET.

9900 base set
base enhancement (signed multiply & div)
9900 ADDITIONS
BYTE STRING OPERATIONS
OTHER OPERATIONS
BIT & FIELD OPERATIONS
MULTIPROCESSOR PRIMITIVES.
DECIMAL OPERATIONS
CONTROL
FLOATING POINT

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

~~3-D 9900~~ ANTIC

REVISIONS IN ANTIC.

ALL MODES LOAD THE SHIFT REGISTER ON THE FIRST

ETC . . .

MAJOR CONCEPT . w/ STAFF CONSENSUS.

TWO PACKAGES.

BASIC BOX WITH CPU.
4K BYTES RAM.
TAPE
ANTIC
STELLA X
488 and/or RS232
GAME CONTROLLERS.

1 PLUG IN ROM SOCKET FOR: a) BASIC
b) SUPER GAMES.
c) PHONE WORD.
d) ~~OTHER~~ - EDUCATIONAL PACKAGE

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WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
COLECO?,

ASIDE) ATARI SHOULD START MAKING ITS SMART TELEPHONE

. PERHAPS, DELETE T88 AND DEFINE A SERIAL BUS - BECAUSE NOTHING NEEDS THE SPEED EXCEPT THE DISK.

STUDY CRU CONCEPT OF 9900 SOME MORE.

(OR USE VIA

⇒ POKEY HAS POTS KEYS SERIAL BUS

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ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COUSIN.

MINIMUM BOX, LSI — COVERS 80-90% OF MARKET

5	CPU (6809, 6502...)	
10	6-8K BYTES OF ROM	MONITOR
16	4K BYTES RAM, PROGRAM, WORKING STORE, SCREEN MAP.	CHAR SET SIMPLE INTEGER BASIC GAME SUBROUTINES.
4	PIA(S) TYPE CONTROL GAME CONTROLLER RANGE SWITCHES.	
6	ANTIC TV NON MOVING O.DEV.	
4.50	TIA-2	OBJECT GENERATION, AUDIO
4.50	POKEY	KBD, POTS, SERIAL I/O EXPANSION. LIGHT PEN.
$ LSI. 50	DECODE DECODER	

PLAYS: SIGMA TYPE GAMES -(4 PLAYER)
: DESERT SOFTWARE
: SIMPLE BASIC
: PROGRAM SOME GAMES.
: COMPATIBLE WITH SLOW I/O DEVICES: TELEPHONE
HOUSE
MUSIC/SPEECH
BURGLER ALARM.
2ND TAPE.

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2ND BOX — PLUGS INTO #1.

BUS EXPANDER.
BIG POWER SUPPLY.
1 OR 2 SLOW PERIPHS.
488 BUS.
RESIDENT DOS ROM.
~~SOCKET FOR PIA + TIMER~~ 8K BYTES of RAM (NO PLUGINS)

WRITER DECOUR/MAHER	DATE 4 AUG	WITNESS	DATE

GAME OR PROJECT
COLLEEN

2ND BOX.

COSTS.

$32	8K RAM.
0	4K ROM. DOS, BOOTSTRAP, ETC.
5	6848 + DRIVERS.
6	DISK CONTROL. ([redacted] or SDLC + P/A)
$48	(DECODER)

+ TWO SLOW DISK DRIVES.

HARDCOPY - USE DAISYWHEEL

OR SOME OTHER WHEEL PRINTER -

~~$[redacted]~~
$400

PERHAPS BUY - OEM.

THE CARRIAGE & PLATEN & RIBBON ASSEMBLY FROM A SCM TYPEWRITER (LOTS OF ELECTRIC TYPEWRITER

ADD SMALL SCANNER (IN A DOT MATRIX PRINTER) AND FACSIMILE TRANSMISSION BECOMES POSSIBLE.

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WRITER	DATE	WITNESS	DATE
DECKER / TAYLOR	7/15/83		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COUPON SYSTEM.

WRITE PROPOSAL IN ENGLISH.

MARKETS: ~~GAME~~ PLAYER
SMALL BUSINESS
TECHNICAL PEOPLE MARKET

CONSIDER USING

82S23 OR 82S123

32 x 8 BIPOLAR PROM

PROBLEMS ~~ASSOCIATED~~ WITH

PROMS - REQUIRES 4 BITS/POINT

AND EXTRA DMA CYCLES. OR

PARALLEL RAM.

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WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
Colloca

~~POSSIBLE~~ POSSIBLE MEMORY MAP:

MAINFRAME	ADD ON
4K RAM	8K RAM (16K?)
8K ROM	4K ROM (8K?)
PIA	DISK I/O
TIA2	6P.A
ANTIC	RS232
POKEY	

4K $	MAINFRAME RAM		
1			
2	ADD ON RAM		
3			
4	MORE RAM?		
5			
		ANTIC	SCREEN MEM, DMA, REFR
		TIA2	MOVING OBJECTS, PADDLE
		POKEY	POTS, KEYBOARD, SERIAL
6	I/O	PIA(S)	TAPE, PANEL, CONTROLLER
7		PIA DISK I/O	DISK CONTROL
8	PLUG IN ROM SPACE	SIO A	
9	(EXTENDED BASIC, OR BUSINESS,	6P.A	IEEE 488
A	OR EXTENDED GAMES, OR PHONE?	ACIA	RS232
B	OR HOME CONTROL/BURGLAR, OR COMPILERS)		
C	DISK MACHINE OS		
D	AND HANDLERS.		
E	MAINFRAME MONITOR, INTEGER BASIC, TAPE HANDLER,		
F	SERIAL HANDLER, CHARACTER SET		

(ADD MEMORY PROTECT VIA P.I.A.'S)

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WRITER Joe Decuir	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC.

THINGS TO DO ON RETURN.

1. PUT ANTIC ON CLEAN MODULATOR AND TRY OUT ON TV TO VERIFY ASPECT RATIOS OF GRAPHICS, CHARACTERS, RESOLUTION OF 20, AND 40 CHARACTER MODES. EXAMINE EFFECTS OF COLORED 40 CHARACTER (140 nsec dot) GRAPHICS. - ON COLOR TV.

DR. MARCUCCI
956-3420

MOVED TO 22ND 9AM.

Meeting of 9th DAT
FULLS
ALCORN
BROWN
VUNCH.

ACCEPTED DAVE'S CONCEPT OF MAINFRAME: TAPE
ANTIC & TIA
D.A & PDICST
CPU
4-8K OS ROM
4K RAM

EXPANSION BOX w/ CARD SLOTS FOR FOM EXTENDED BASIC ETC.

DATA CONVERTIBILITY NOT REQUIRED.

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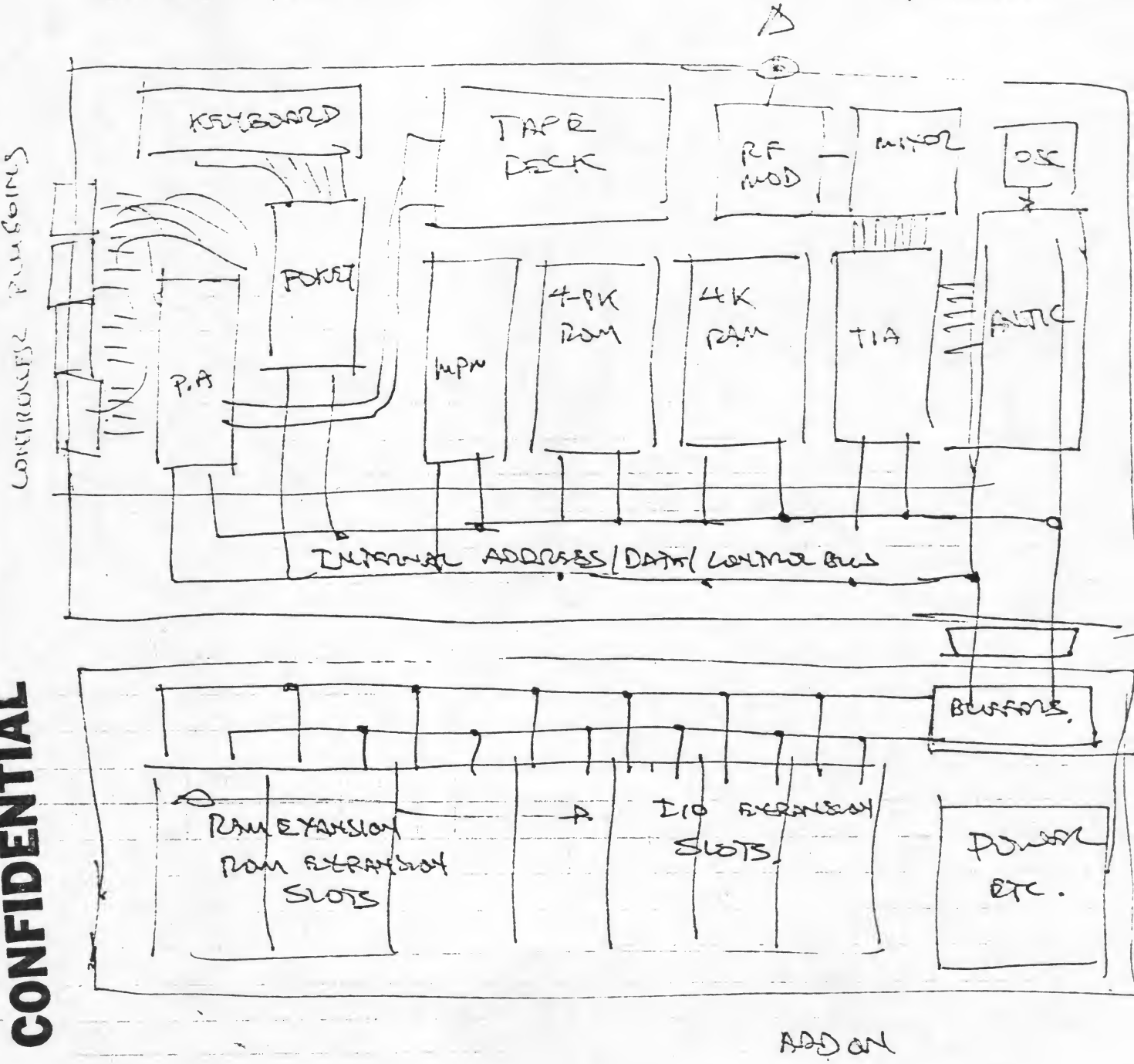
WRITER DRELLER	DATE	WITNESS	DATE

ATARI

GAME OR PROJECT
COLLEEN

JAY'S PROPOSAL



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BASICALLY ACCEPTED
BY BROWN, ACCORN, ELLIS, MURICH

WRITER DRAWN	DATE 9/7/76	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN

STEVE WANTS TO SELL CAPABILITY

BEING TO BUILD THINGS IN IF IT'S CHEAP -
KEEP TOTAL NUMBER OF DIFFERENT COMPONENTS DOWN.
DON'T NICKLE AND DIME THEM TO DEATH

DIFFERENCES:

1) ADD ~~SIO~~ SERIAL I/O EXPANSION AND SINGLE CARTRIDGE EXPANSION

2) 2ND UNIT IS SINGLE PACKAGE W/DUAL FLOPPYS, RAM, ROM, AND 488 TYPE ~~GPIB~~ I/O — RATHER THAN AN UNLOAD MOTHERBOARD EXPANSION BOX

OUTLINE OF PROPOSAL

1) MAINFRAME IS ENTERTAINMENT MACHINE
VIDEO GAMES
DOS II
PHONE
HOUSE CONTROL
MUSIC
SIMPLE PROGRAMMING.
SMART TERMINAL

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		WITNESS	DATE

GAME OR PROJECT
COLLEEN.

2) 2ND MACHINE IS FOR SERIOUS WORK.
~~BOOT~~ DUAL DISKS, RAM & ROM,
TO SUPPORT SERIOUS PROGRAMMING
SOPHISTICATED PERIPHERALS.

COMPILERS
SMALL BUSINESS DP
WORD PROCESSING
SCIENTIFIC NUMBER CRUNCHING
(SIMULATION, COMPUTER AIDED DESIGN,
STATISTICAL ANALYSIS)
LOCAL PROCESSING FOR
~~SMALL~~ LARGE COMPUTER.

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STUFF TO BRING UP: VIDEO MODULATOR?
COLOR TV.

COMPLEX PROGRAM
LISTING

PICKED UP AT PALO ALTO AIRPORT
SUNDAY NIGHT

STEVE'S FOLKS
415-368-8876
1200 WOOD CT.

WRITER DECUIR	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
PAL STELLA

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GOT PAL COLOR WORKING!!

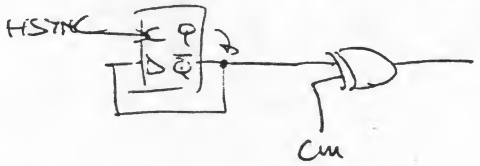
THINGS THAT HELPED:

1) TUNE PAL COLOR OSCILLATOR TO 4.433613 MHZ.

2) PUT RF AMPLIFIER ON VIDEO OUTPUT

3) FINER TUNING ON TV.

4) CHANGING POLARITY OF FLIP FLOP OUTPUT FOR PHASE ALTERNATION



5) ADJUSTING DELAY LINE PROP DELAY CAREFULLY.

RUNNING WITH HSYNC =

$$228 \times \frac{5}{4} \times \frac{1}{4.433613\ \text{MHZ}}$$

NO FUNNY EFFECTS NOTICED ON TANKS OR ON MISSILES.

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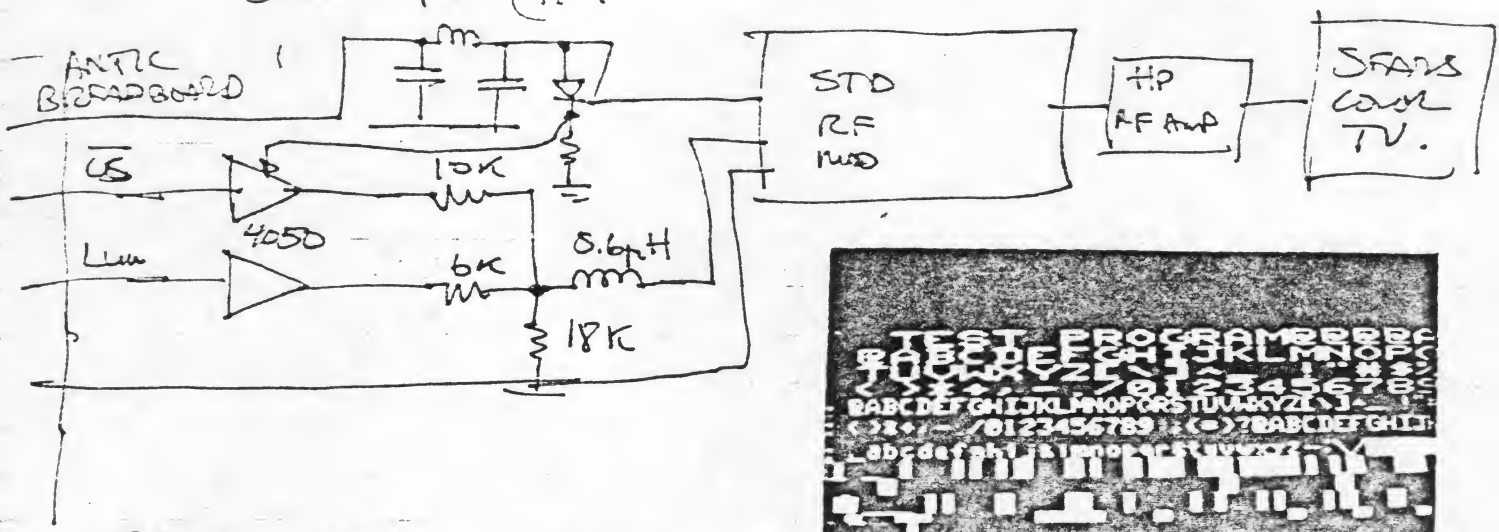
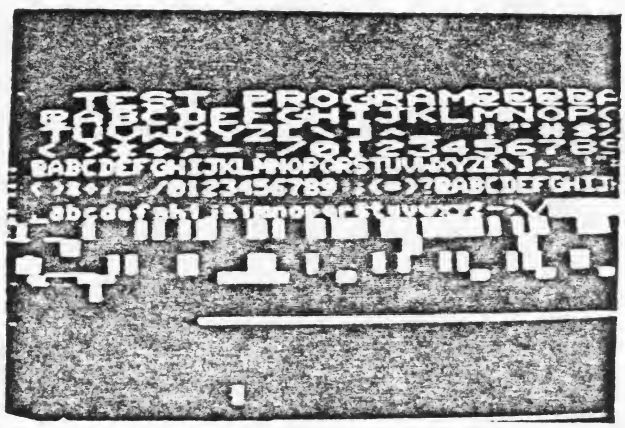
GAME OR PROJECT
ANTIC.

AUGUST 15, 16, 17, 18. WORKED ON ANTIC IN GLASS VALLEY.

MONDAY: INSTALLED RF MODULATOR

PUT 40 CHAR/LINE ON SCREEN. IN BLACK AND WHITE, ON A SEARS COLOR TV (15"?)





~~READ~~ VIDEO SUMMING,

RF INTERFERENCE ISOLATION,

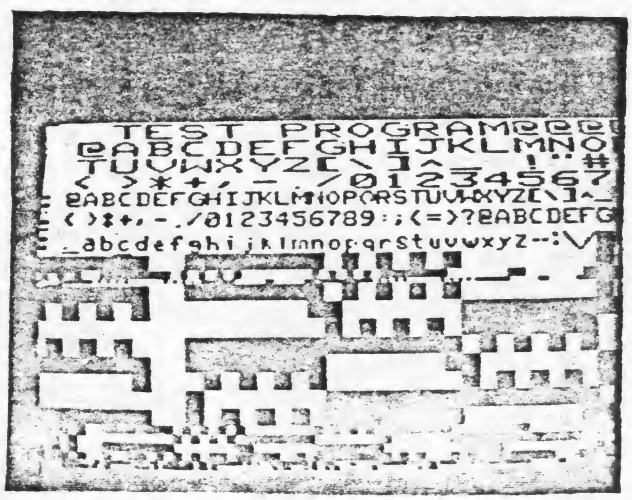
AND RF AMPLIFICATIONS IS

BASICALLY IDENTICAL TO

STELLA, W/ TWO EXCEPTIONS:

1) NO COLOR BURST,

2) RF AMP USED TO ~~GEN~~ REDUCE ~~NOISE FROM~~ INTERFERENCE FROM BREADBOARD AND PPP-11 COMPUTER NEARBY.



WRITER	DATE	WITNESS	DATE
JEFF DRELLA	12 AUG 77		

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC BREADBOARD

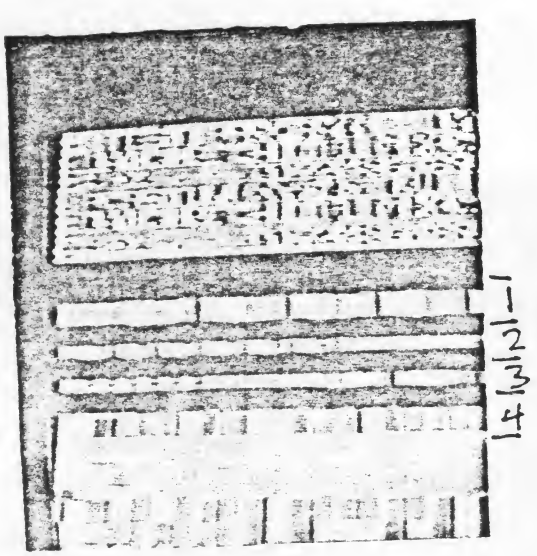
~~SIMULATION~~

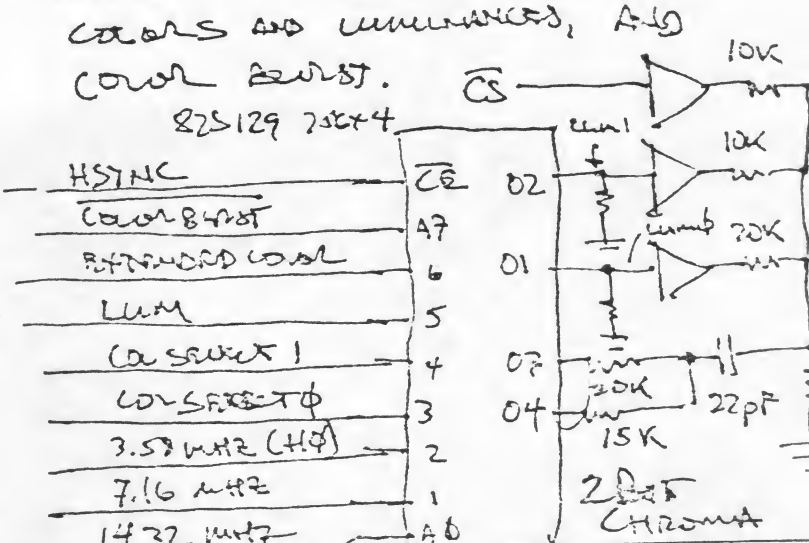
COMMENTS: AS CAN BE SEEN FROM POLAROID (SX-70) PHOTOS ON PREVIOUS PAGE, CHARACTERS ARE SHARP IN BLACK AND WHITE. DEPENDING ON CONTRAST, SOMETIMES BLACK ON WHITE LOOKED SHARPER THAN WHITE ON BLACK.

SMALLEST CHARACTERS ARE 40 (8x8)/LINE.
DOT CLOCK = 2x NTSC COLOR = 7.16 MHz.
(COLOR BURST NOT ON!)

TUESDAY 16 AUGUST

ADDED COLOR, USING 14MHz AND SUB HARMONICS TO GENERATE COLOR WITH A PROM. OTHER INPUTS WERE USED TO SELECT COLORS AND LUMINANCES, AND COLOR BURST.





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WRITER	DATE	WITNESS	DATE
JCS DECKER	8/16/77		

GAME OR PROJECT
ANTIC BREADBOARD.

AS CAN BE SEEN IN THE PHOTO, COLORS WORK. IN THE HORIZONTAL BANDS 1, 2, 3, 4. SCREEN MAP MODES ARE TESTED.

BAND 1 IS THE 40 BIT MODE:
10 DMA'S/LINE ⇒ 5 × 8 × 2 = 40 × 2 BITS
= 40 POINTS, 4 COLOR CLOCKS × 8 LINES × 4 COLORS. (STELLA PF RESOLUTION)

BAND 2 IS THE 80 POINT MODE:
20 DMA'S/LINE ⇒ 10 × 80 × 2 = 80 × 2 BITS.
EACH POINT 2 COLOR CLOCKS × 4 COLORS × 8 LINES
(APPROXIMATELY FAIRCHILD RESOLUTION)

BAND 3 IS 3 REPETITIONS OF THE 160 POINT MODE:
40 DMA'S/LINE ⇒ 20 × 80 × 2 = 160 × 2 BITS.
EACH POINT 1 CLOCK × 2 LINES × 4 COLORS
(STELLA OBJECT RESOLUTION).

BAND 4 SAME AS BAND 1.

AT THE TOP OF SCREEN, 20 AND 40 CHARACTER LINES ARE DISPLAYED W/ COLORS. NOTE THAT THE CHROMA CARRIER MIXES WITH THE LUMINANCE WITH PECULIAR RESULTS. THIS BEARS FURTHER STUDY (WHAT IF COLOR BURST WAS ON, BUT NO COLOR CARRIER DURING THE LINE?)

WRITER JOE DECUIR	DATE 12 AUG 77	WITNESS	DATE

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ATARI ENGINEERING LOG SHEE

GAME OR PROJECT

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$\frac{9.7+7.4}{2} = \frac{17.3}{3} = 5.55$

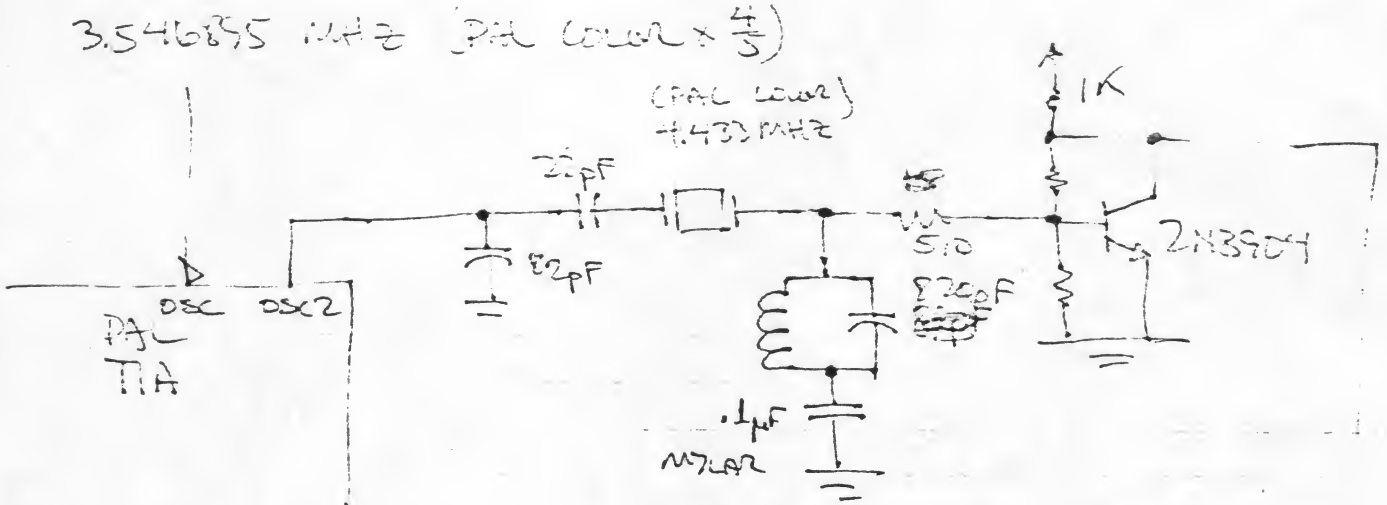
SENSITIVITY & FREQUENCY.

COLOR MODULATOR 4.433618 75

WRITER	DATE	WITNESS	DATE

GAME OR PROJECT
CYNTHIA

NILES' CKT FOR PAL COLOR.



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WRITER JOE DECUIR	DATE 2.6.80T	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC

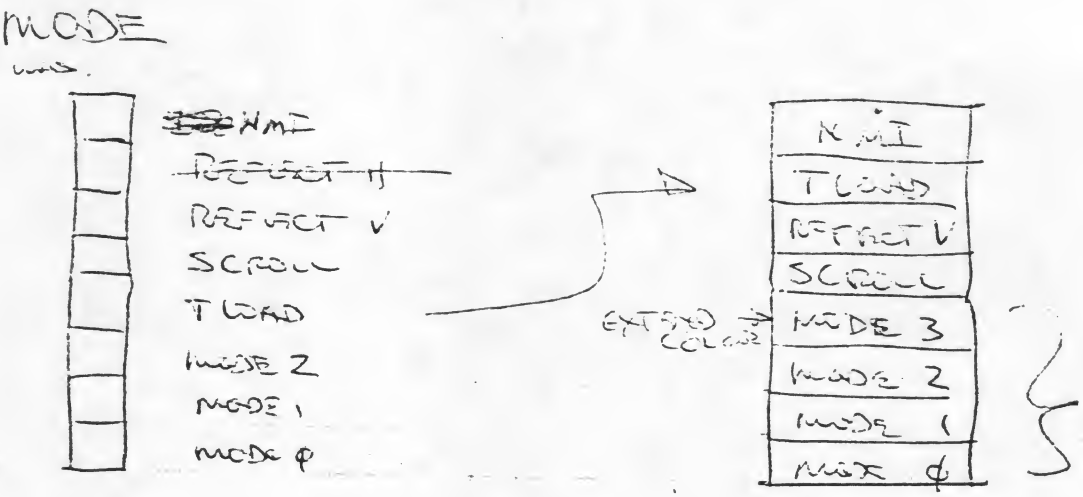
MODE		EXTENDED COLOR 0	EXTENDED COLOR 1
000		BLANK - (1-8 LINES)	SAME
001	(1 DMA LINE)	20 CHAR/LINE 2 COLOR BITS x 8 BITS/CHAR. 2^6 CHAR + 2 COLOR BITS. 8 LINES x 8 CLOCKS.	20 CHAR/LINE 2 COLOR BITS / POINT. 2^7 CHAR + START ADDR (5 D.MA/LINE)
010		40 CHAR/LINE 2^7 CHAR + INVERT VIDEO 10 LINES x 4 CLOCKS (4 D.MA/LINE)	SAME
011		SPARE	SPARE
100		SPARE	SPARE
101		MEM MAP 40 BITS/LINE x 8 LINE (5 DMA/LINE)	MEM MAP 40 x 2 BITS/LINE x 8 LINES (10 DMA/LINE)
110		MEM MAP 80 BITS/LINE x 4 LINES (10 DMA/LINE)	MEM MAP 80 x 2 BITS/LINE x 4 LINES (20 D.MA/LINE)
111		MEM MAP 160 BITS/LINE x 2 LINES (20 DMA/LINE)	MEM MAP 160 x 2 BITS/LINE x 2 LINES. (40 D.MA/LINE)

CONFIDENTIAL

GAME OR PROJECT

ANTIC

CONFIDENTIAL



MODE SUMMARY TO DATE

CLOCK = 3.58 MHz cycle.

CODE?	MODE	DESCRIPTION	ELEMENT SIZE
	BLANK	1 ≤ N ≤ 8 LINES BLANK	N LINES.
	20 CHAR 1	8×8×1 CHAR × 2 COLOR BITS	8 LINES × 8 CLOCKS
	20 CHAR 2	" "	8 PAIRS × 8 CLOCKS
	20 CHAR 3	8×8×2 CHARACTER	8 LINES × 8 CLOCKS
	20 CHAR 4	" "	8 PAIRS × 8 CLOCKS
	40 CHAR	8×8×1 CHAR × 1 INVERT BIT.	10 LINES × 8×½ CLOCKS.
	40 CELL 1	(1 BIT SQUARES)	8 LINES × 4 CLOCKS
	40 CELL 2	(2 BIT SQUARES)	
	80 CELL 1	1 BIT SQUARES	4 LINES × 2 CLOCKS
	80 CELL 2	2 BIT SQUARES	
	160 CELL 1	1 BIT SQUARES	2 LINES × 1 CLOCK.
	160 CELL 2	2 BIT SQUARES	

WRITER [illegible] DATE WITNESS

ATARI ENGINEERING LOG SHEET

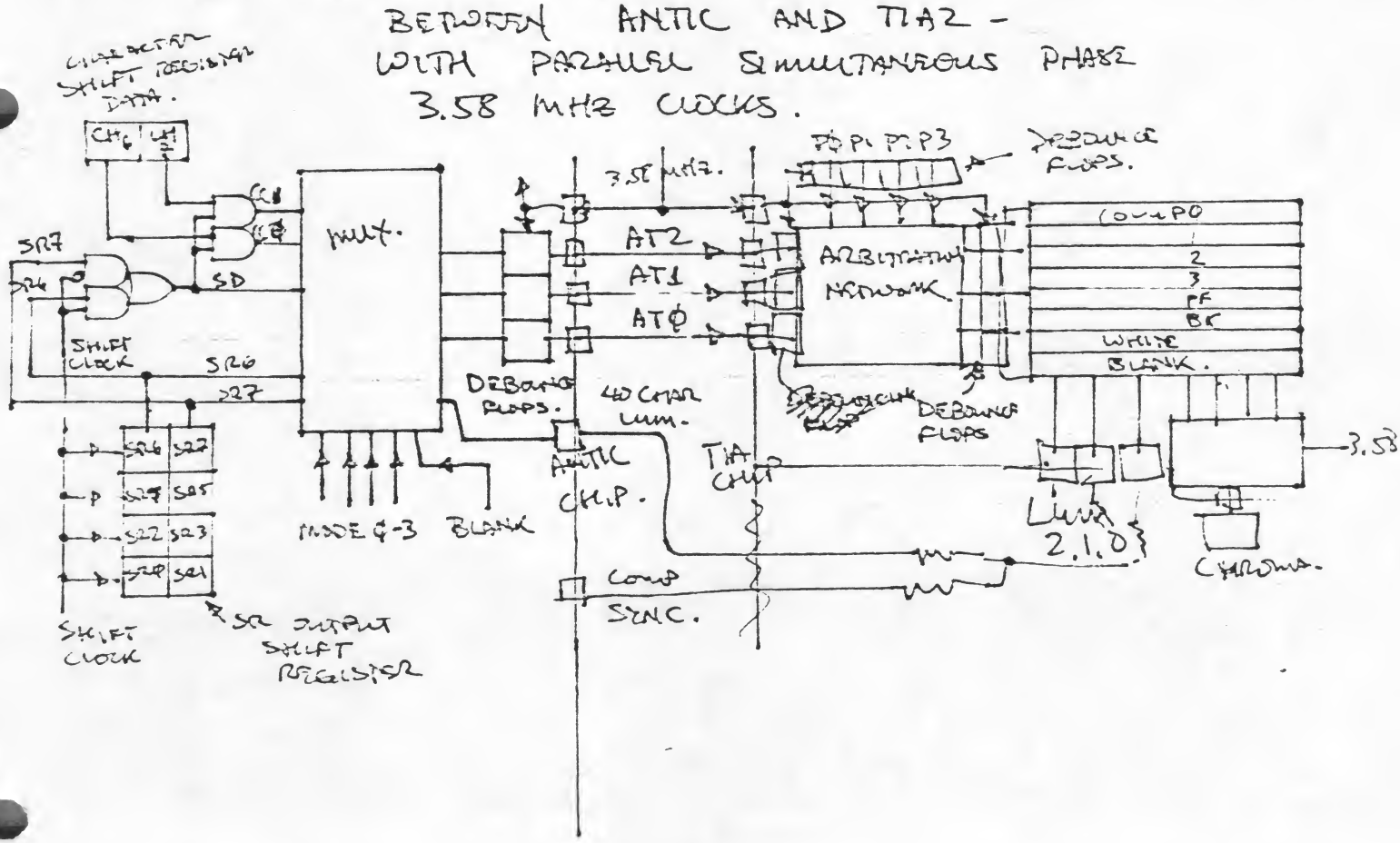
CONFIDENTIAL

GAME OR PROJECT
ANTIC VIDEO COMMUNICATION TO TIA2

6 COLOR LUM REGISTERS IN TIA2.

AT2	AT1	AT0		
1	0	0	COLUM P0	P0, 20 CHAR x 4 COLOR
1	0	1	COLUM P1	P1, 20 CHAR x 4 COLOR
1	1	0	COLUM P2	P2, 20 CHAR x 4 COLOR, EXTENDED COLOR
1	1	1	COLUM P3	P3, 20 CHAR x 4 COLOR, EXTENDED COLOR
0	0	1	COLUM PF	PLAY FIELD 2 COLOR, BOARD, EXTENDED COLOR
0	0	0	COLUM BK	DEFAULT - " " " , BLANK MODE
0	1	0	FORCE WHITE	40 CHAR MODE
0	1	1	FORCE BLANK.	HOR V BLANKING

3 COMMUNICATION LINES BETWEEN ANTIC AND TIA2 - WITH PARALLEL SIMULTANEOUS PHASE 3.58 MHZ CLOCKS.



GAME OR PROJECT

(BLANK)

CONFIDENTIAL

EXPANDED ATARI BASIC CARTRIDGE.

GOO FOR MAINFRAME

GOO FOR MAINFRAME COMPUTER ENVIRONMENT

48 K RAM.

4K ROM.

4K BANK EXCHANGABLE FOR ROM'S.

MULTIPLEXED DYNAMIC RAMS INTERNAL.

3 JACKS ON BACK FOR TAPES AND 4C.
(IDENTICAL IN APPEARANCE!)

ONE EXPANSION BUS CONNECTOR. (40 PIN)

300 BAUD TAPE FORMAT.

GRAPHICS ARE BLACK & WHITE
GRAPHICS, 1 LEVEL. 160×64

OR 320×192 GRAPHICS.

HELP MONITOR THAT YOU CAN CALL
BY ESCAPE KEY.
TAPE LOADED PROGRAMS ARE
WRITTEN IN BASIC. ~~ALLOWS~~
ALLOWS YOU TO LIST THE PROGRAM.

EXTERNAL TRANSFORMERS. (ON BOARD) REGULATED
CAPACITORS. (NO AC INTERNAL.

NON-VOL. SAVE IN

USE EPAC
IN SERVICE MANUAL

WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

6502

ERROR SHEET

SYNERTEK — BILL BOUSE.

ERROR PROC — BEN BRUNER

JERRY DRUMEY. — MICRO ASSOC

LOOK AS SYNERTEK'S LIST FIRST.

SINGLE HALT LINE -
HALTS PROCESSOR AND
TRI STATES BUSES.

ASK FOR A SPECIFICATION
BETWEEN φ0 IN, φ1 OUT, φ2 OUT.

P: C, V, I, Z, N, D, B.

MUST BREAK TO SERVICE
VECTOR - UNLOAD ADDR BIT.

AND HALF CARRY

ENABLE AUTO INCREMENT.

CONFIDENTIAL

GAME OR PROJECT

2509

JMP DS2

JMP DS2

JMP DS2

JMP

DS2

TPA. P

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
GREEN

JAY'S REPORT FROM RADARO

4K RAM.
ROM CARTRIDGE SLOT. 8K OR LARGER.
CODE (UNDER COPY)
PORTS & RESIDENT KEYBOARD.
VIA & SERIAL EXPANSION.
64K RESIDENT ROM'S
NO RESIDENT OPERATE.
(RAM CARTRIDGE)
ANTIC & RESIDENT TIA.
2 CASSETTE JACKS -
W/ MOTOR START STOP.
AUTOMATIC REWIND?
LIGHT PEN.
AUDIO AND DIGITAL ON TAPE.

CONFIDENTIAL

OTA SAYS 6509 IS

816 MAYBE, BECAUSE OF TIME.

WHAT IS SENSITIVITY OF SCHEDULE VS FEATURES.

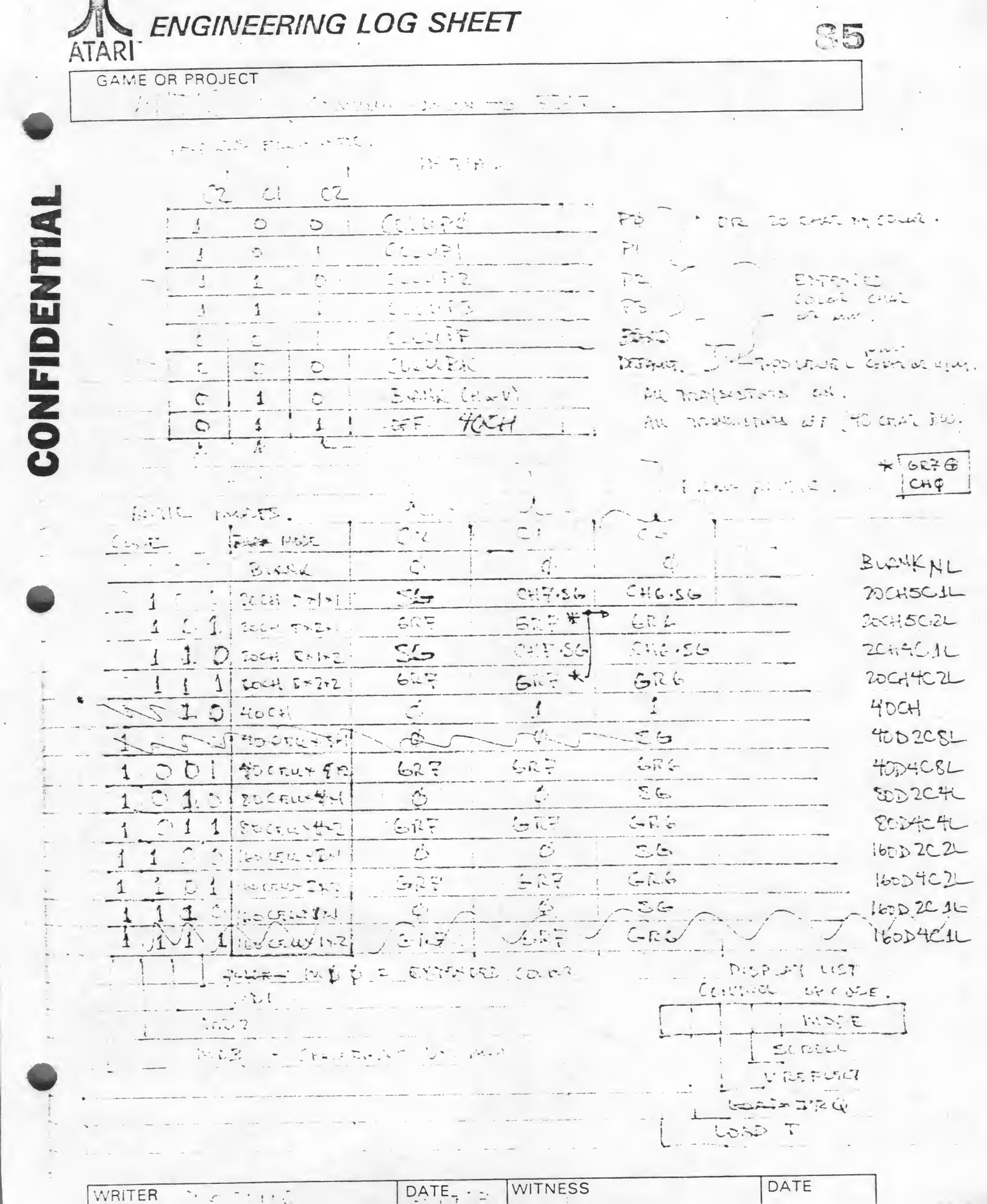
HOW FAST CAN WE BRING UP OTHER VENDORS.

PROBES CANNOT BE
HOW ABOUT OTHER ~~HOSE~~ VENDORS
LIKE ANC AND AMI?

	DATE	WITNESS	DATE

GAME OR PROJECT

CONFIDENTIAL



WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT

ANTIC — DELUXE ADDRESS GENERATOR.

CONFIDENTIAL

BC [7 6 5 4 3 2 1 0] — BASE POINTER FOR CHARACTERS

SR [7 6 5 4 3 2 1 0] — OUTPUT OF CHARACTER BUFFER.

DL [15 7 6 5 4 3 2 1 0] — DISPLAY LIST POINTER.

T [15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0] — MEMORY SCANNER COUNTER

LATCH. | BINARY DOUBLE COUNTER.

A [2 1 1 1 0] — BLOCK 3 BIT LINE-DOWN COUNTER.

H [8 7 6 5 4 3 2 1 0] — HORIZONTAL SYNC COUNTER

V [8 7 6 5 4 3 2 1 0] — VERTICAL SYNC COUNTER

R/L RIGHT-LEFT BYTE SELECT FOR ~~8~~ CHAR 20 CHANNEL 4 COLOR MODE. — DERIVED FROM H2

TYPE OF CYCLE.	MODE	ADDRESS BUS															
BLANK N	0 0 0 0																
40 CH	0 0 1 0	BC7	6	5	4	3	BC2	SR6	5	4	3	2	1	0	Δ2	1	Φ
20 CH 5COL 1L	0 1 0 0	BC7	6	5	4	3	2	BC1	SR5	4	3	2	1	Φ	Δ2	1	Φ
20 CH 4COL 1L	0 1 0 1	BC7	6	5	4	BC3	SR7	6	5	4	3	2	1	R/L	"	"	"
20 CH 5COL 2L	0 1 1 0	BC7	6	5	4	3	2	BC1	SR5	4	3	2	1	SR0	"	"	"
20 CH 4COL 2L	0 1 1 1	BC7	6	5	4	3	SR7	6	5	4	3	2	1	R/L	Δ2	1	Φ
40 CELL 2COL 8L	1 0 0 0	T LATCH					T COUNTER T11 – TΦ										
40 CELL 4COL 8L	1 0 0 1	T5	14	13	12		"										
80 CELL 2COL 4L	1 0 1 0	"					"										
80 CELL 4COL 4L	1 0 1 1	"					"										
160 CELL 2COL 2L	1 1 0 0	"					"										
160 CELL 4COL 2L	1 1 0 1	"					"										
160 CELL 2COL 1L	1 1 1 0	"					"										
160 CELL 4COL 1L	1 1 1 1	T5	T4	T3	T2	T1	"										TΦ
REFRESH		0	0	0	0	0	0	0	0	14	13	12	11	10	H3	H2	
MODE FETCH.		DC15	14	13	12	11	10	9	DC8	7	6	5	4	3	2	1	DC0
OBJECTS		OBJ15	OBJ14	13	12	11	10	P3/9	H	OBJ8	6	5	4	3	2	1	OBJ0

T.A OBJECTS
TIA VIDEO:

TP0 ~
TP1 } OBJECTS GENERATED.
TP2
TP3
TBD } BOARD GENERATED

ANTIC VIDEO

DECODES FROM ANTIC VIDEO

APF — CODE # 1 — 2 COLOR SCREEN AND. 4 COLOR SCREEN AND
AP0 — CODE 4 — 5 COLOR CHAR OR 4 COLOR CHAR
AP1 — CODE 5 — " "
AP2 — CODE 6 — 5 COLOR CHAR, 4 COLOR CHAR, OR 4 COLOR S
AP3 — CODE 7 — " "

ANTIC VIDEO MODES ARE EXCLUSIVE —
SO NO collisions need be detected among them.
the board generator can be classed with the playfield. — SINCE NO collisions are of significance expected between it and antic generated objects.

	AP0	AP1	AP2	AP3	TBD INT	APF	AP1	AP2	AP3
AP3	—	O	O	O		X	X	X	—
AP2	O	—	O	O		X	X	—	
AP1	O	O	—	O		X	—		
AP0	O	O	O	—		—			
TBD + APF	O	O	O	O	—				
TP3	O	O	O	—					
TP2	O	O	—						
TP1	O	—							
TP0	—								

20 COLLISIONS BETWEEN 4 TIA OBJECTS AND 5 DIFFERENT EXCLUSIVE DECODES.

6 MUTUAL COLLISIONS AMONG 4 T.A MOVING OBJECTS.

WRITER DECKER	DATE 2/21/77	WITNESS	DATE

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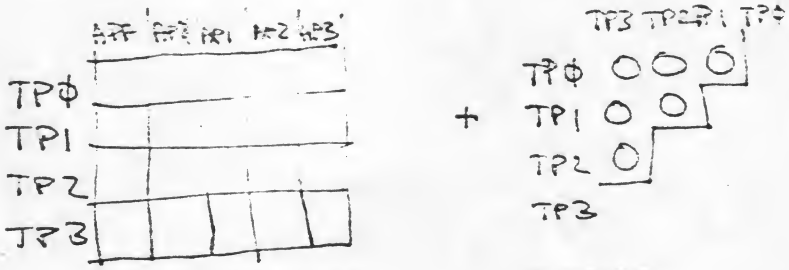
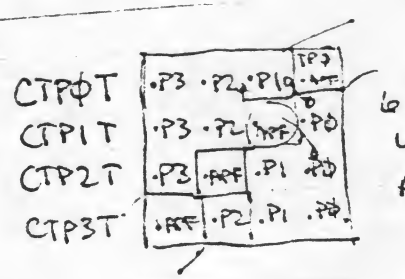
GAME OR PROJECT
ANTIC - T.A Collisions - cont.

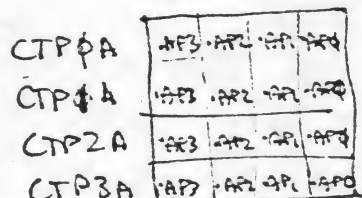
CONFIDENTIAL

26 COLLISIONS.



?





LOOKS LIKE 32 BITS.
OR 4 BYTES,
OR 16 PAIRS.

BIT7 BIT6

16 PAIR CONFIGURATIONS.

· APF		· APØ
TPØ · TPI		TPØ · API
· TP2		· AP2
· TP3		· AP3
· TPØ		· APØ
TPI · APF		TPI · API
· TP2		· AP2
· TP3		· AP3
· TPØ		· APØ
TP2 · TPI		TP2 · API
· APF		· AP2
· TP3		· AP3
· TPØ		· APØ
TP3 · TPI		TP3 · API
· TP2		· AP2
· APF		· AP3

OR

TPØ · APF		TPØ · AP
TPI TPØ		TPI ·
TP2 TPØ		TP2 ·
TP3 TPØ		TP3 ·
TPØ TPI		TPØ · A
TPI APF		TPI ·
TP2 TPI		TP2 ·
TP3 TPI		TP3 ·
TPØ TP2		TPØ ·
TPI TP2		TPI ·
TP2 APF		TP2 ·
TP3 TP2		TP3 ·
TPØ TP3		TPØ ·
TPI TP3		TPI ·
TP2 TP3		TP2 ·
TP3 APF		TP3 ·

DATE

GAME OR PROJECT

ANTIC - THE PRINCIPAL DISPLAY

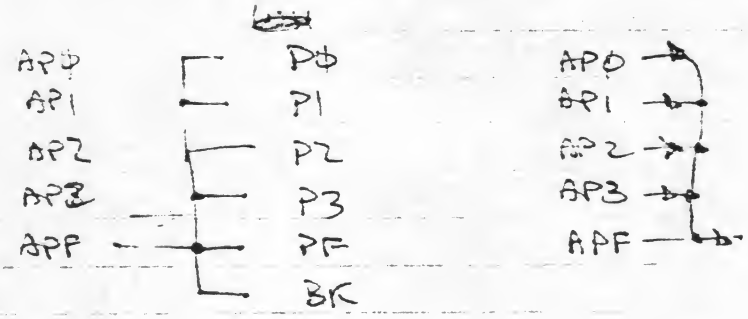
CONFIDENTIAL

(CONTROL BITS.

PFP PLAYFIELD PRIORITY. -

P0		PF
P1		P0
P2	VS	P1
P3		P2
PF		P3
BK		BK

ATC ANTIC COLOR.



WRITER	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
T.A2 PINS AND ADDRESSES

CONFIDENTIAL

A TIA2 CONTAINS

4 8 BIT LATCHES
⇒ 6 COLOR/LUMINANCE REGISTERS
COLLISION LATCHES

WRITE ADDRESSES

	COLUPϕ, 1, 2, 3	4
	GRPϕ, 1, 2, 3	4
	HPOSPϕ, 1, 2, 3	4
	NUSIZPϕ, 1, 2, 3	4
+ 16 COLLISION READ ADDRESSES.	VDELPϕ, 1, 2, 3	4
		20
	COLUPF	
	COLUBK	
	CTRLPF	
	CTRLBD	
	CXCLR	5
		25

< 32

PINS	VSS, VCC	2
	CLK (3.58)	1
	SYNC (ANTIC)	1
	R/W, ϕ2	2
	Dϕ-D7	8
	Aϕ-A4	5
	$\overline{CS}$	1
	ANϕ, 1, 2	3
	LUMϕ, 1, 2	3
	CHROMA, DEL	2
		28 !!!

WRITER	DATE	WITNESS	DATE
JOSEPH DECUIR	2 OCT		

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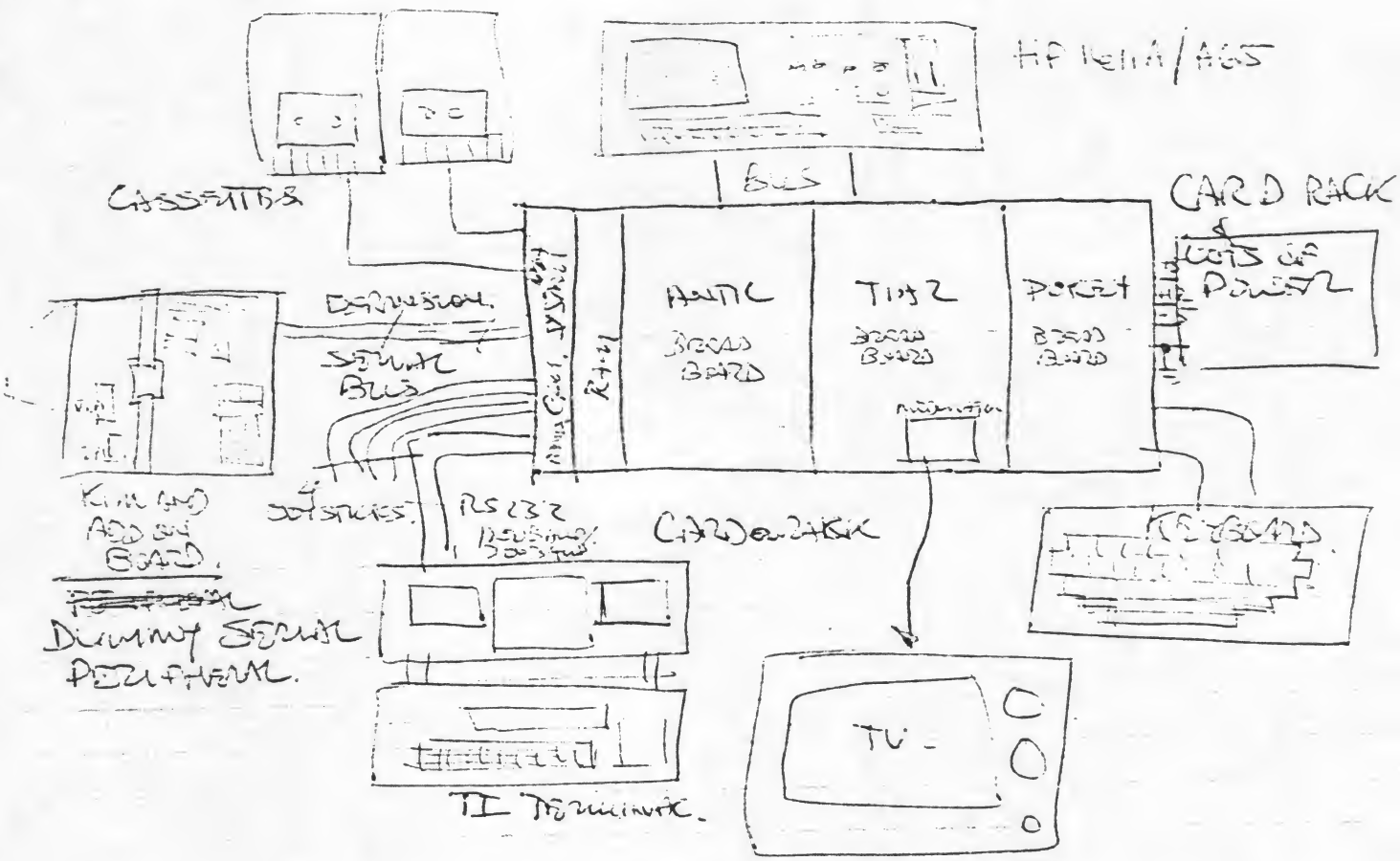
GAME OR PROJECT

DEVELOPMENT SYSTEMS FOR COUSIN

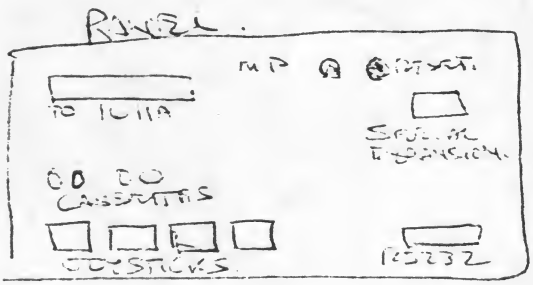
CONCEPT:

FOR CART DEVELOPMENT.
AND EARLY SOFTWARE DEVELOPMENT:

2 COMPLETE MACHINES.



16114A FOR LOGIC ANALYSER, DISASS.
TI FOR LOAD/STORE TAPES.



SYSTEM BOARD INCLUDES.
CPU.
BUS BUFFERS.
VIA FOR JOYSTICKS, TAPE I/O
SERIAL PORT
TAPE I/F

16114A FOR TI IN IMAGE
PROMS WITH DEVELOPMENT
MONITOR (IE: LOAD BUG ON

WRITER	DATE	WITNESS	DATE
JOE DILLER	12 OCT.		

ATARI ENGINEERING LOG SHEET

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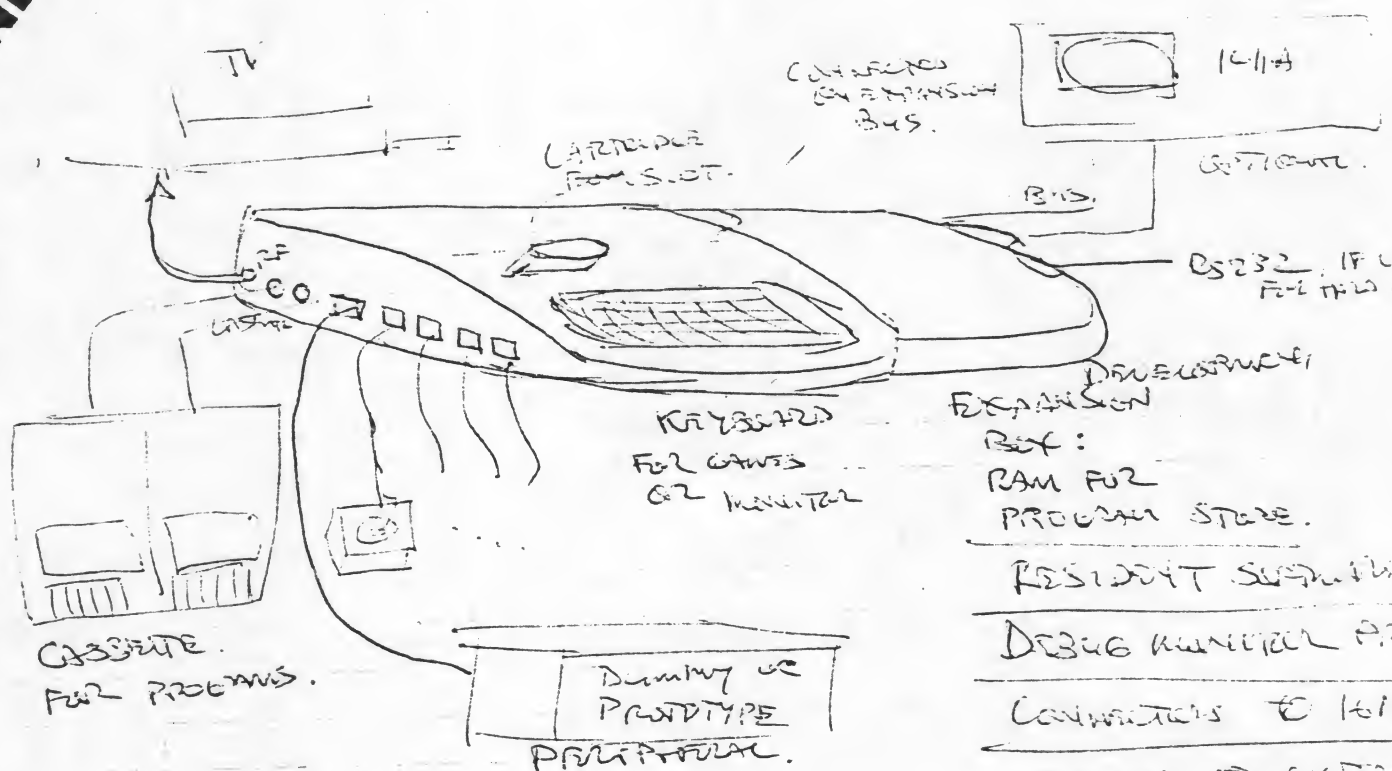
GAME OR PROJECT
COLECO DEVELOPMENT SYSTEM

CONCEPT FOR PRODUCTION SOFTWARE DEVELOPMENT UNITS.



BUILD A WORKING COLECO UNIT.

ONTO THE EXPANSION BUS. ADD A BOX THAT ALLOWS LOADING AND DEBUGGING OF APPLICATIONS PROGRAMS. — USE RESIDENT KEYBOARD AND TV SCREEN FOR COMMUNICATION W/ DEBUG MONITOR.

GAME OR PROJECT

ANTIC, POKEY

CONFIDENTIAL

PINOUTS. ANTIC

2	Vcc, Vss	POWER	POWER AND CLOCKS.
1	OSC	3.58 CLOCK	
2	$\phi 1$ $\phi 2$	CLOCKS TO MPU.	
2	TSC, RW	BUS CONTROL	PROC. SIGNALS
1	$\overline{AINT}$	INTERRUPT OUT (TO MMU)	TO MMU
1	$\overline{CS}$	REGISTER CHIP SELECT.	SIGNALS
8	DBϕ-DB7	DATA BUS.	
16	ABϕ-AB15	ADDRESS BUS	
1	SYNC,	SYNC CONTROL TO DAC	VIDEO.
3	ANϕ,1,2	VIDEO TO DAC	
2	CSYN, LPC	COMPOSITE SYNC, 4Q CH. LUM OUT.	
35	PWRS		
1	LP.	LIGHT PEN ?	
40	~~[illegible]~~	$\phi 2$ IN POKEY.	

PINOUTS. POKEY.

2	VSS, Vcc	POWER	POWER AND CLOCKS
1	$\phi 2$	CLOCK.	
1 ?	SYNC	HORIZONTAL FROM ANTIC.	
1	$\overline{PINT}$ (OD)	POKEY INTERRUPT REQUEST.	
2	$\overline{CS}$	CHIP SELECT	INPUT BUS. SIGNALS.
4	Aϕ-A3	ADDRESS INPUTS	
8	Dϕ-D7	DATA BUS	
1	R/W		
8	Pϕ-P7	POT INPUTS.	I/O
8	KRϕ-KR7	KEYBOARD INPUTS	
12 { 3	KSϕ,1,2	ENCODED KEYBOARD SCAN OUTPUTS.	
12 { 1	AUD	AUDIO	
40	PWRS.		

WRITER	DATE	WITNESS	DATE
JOE DELLINGER	OCT 77		

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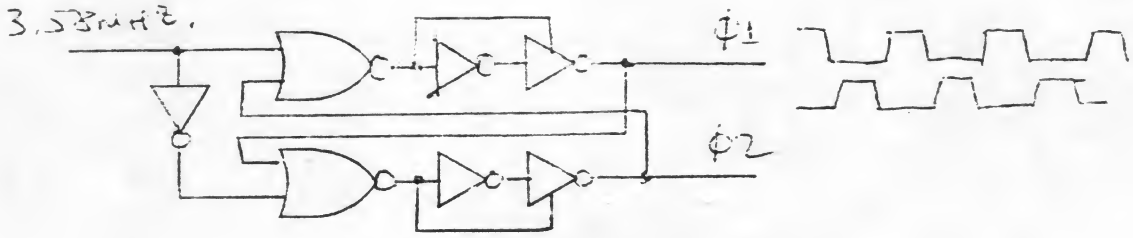
GAME OR PROJECT

ANTIC.

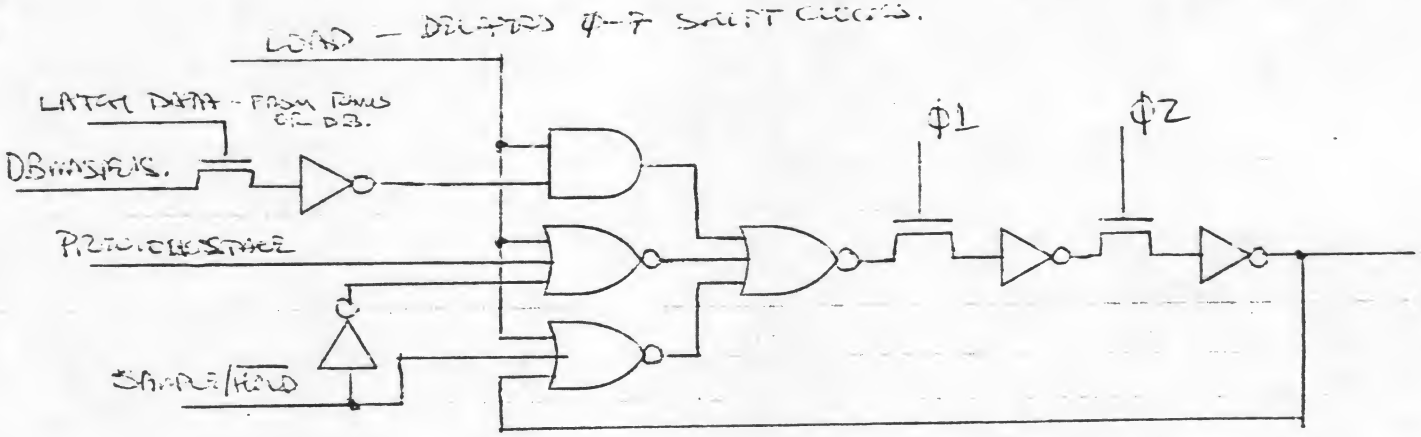
CONFIDENTIAL

2 CELLS

ϕ $\phi 1$, $\phi 2$ SQUARE PULSES USED IN ANTIC



OUTPUT SHIFT REGISTER CELL.



GAME OR PROJECT

ANTIC 'COUSIN'.

CONFIDENTIAL

CONVERSATION W/ JOHN

ANTIC PINOUT.

DON'T PUT LIGHT PEN ON ANTIC.

DON'T CONTAIN SEPARATE SYNC TO TIA —
US CSYNC PIN —
AND BUFFER INTERNALLY WITH ONE
USED TWO.

→ ANTIC HAS 28 PINS.

→ 2 PINS FOR DMA GRANT, DMA REQUEST.

SIENE SUGGESTS SCROLLING

WHOLE SCREEN BY SHIFTING

SYNC AND BLANK.

LEAVE OUT DIRECT SCROLLING.

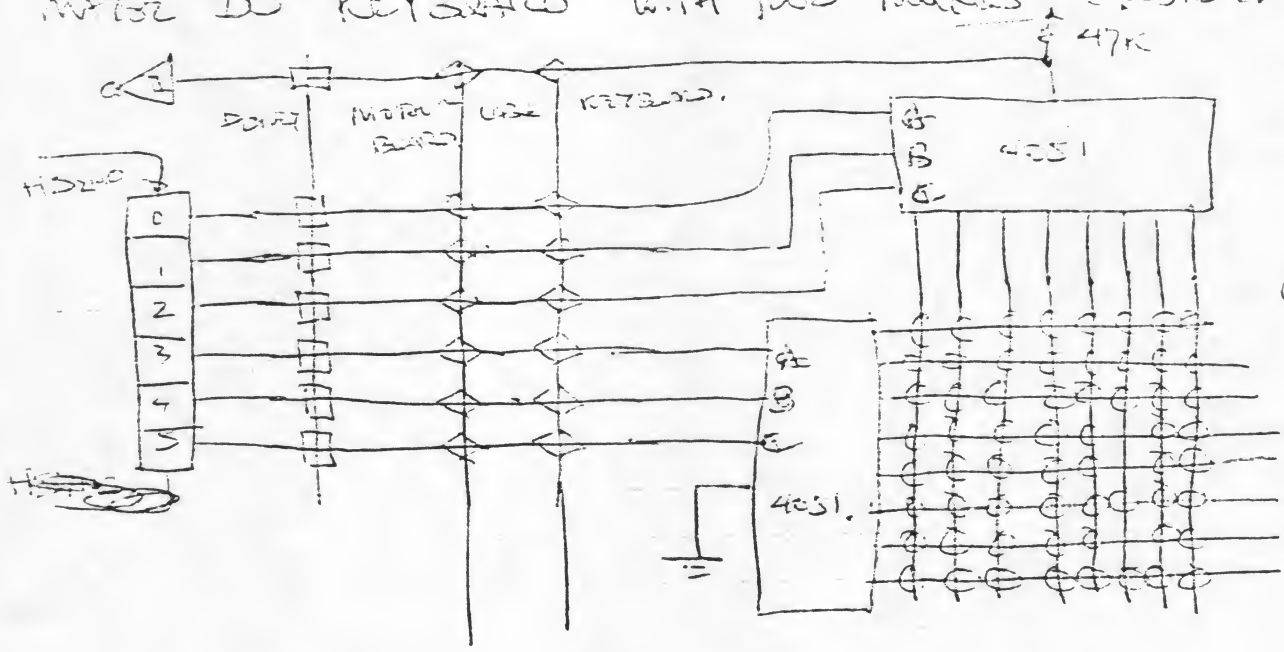
ATARI

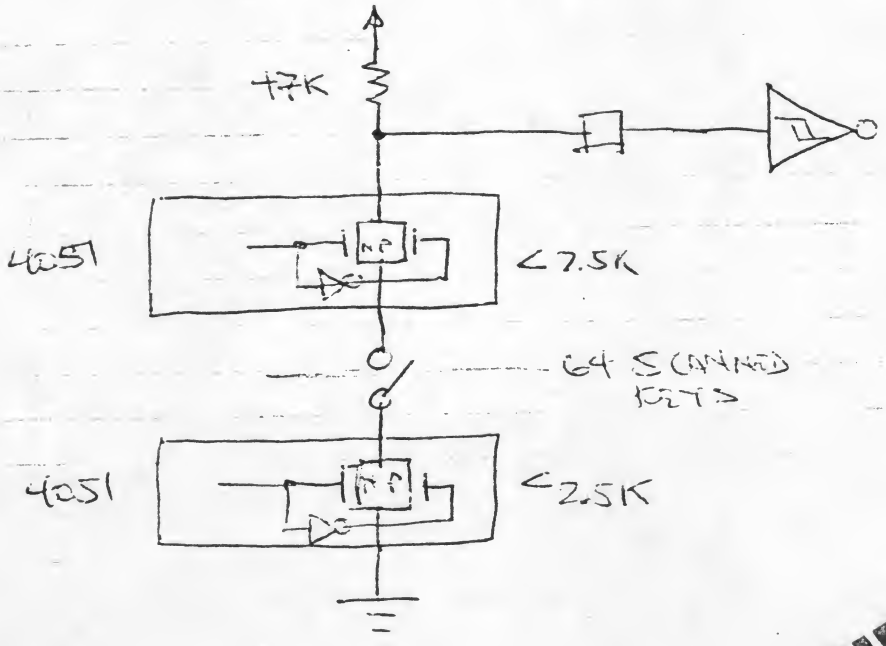
ENGINEERING LOG SHEET

GAME OR PROJECT

POKEY - KEYBOARD

WIRE DO KEYBOARD WITH TWO MUXES - 4051B CMOS





$\frac{5}{5+47} = \frac{5}{52} \times 5.0 \text{ V} \approx$

CONFIDENTIAL

	DATE	WITNESS	DATE

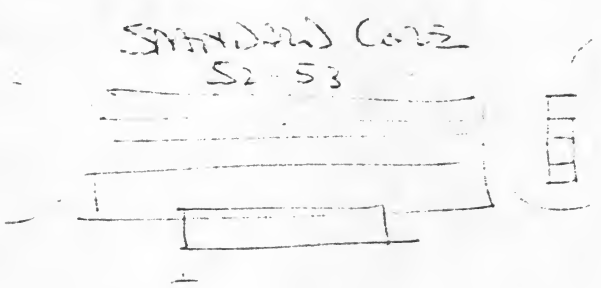
GAME OR PROJECT

~~Double~~ KEYBOARD MOUSE

CONFIDENTIAL

TEST DOCUMENT.

STANDARD CART
52 - 53



4/SIDE
2/SIDE
1/SIDE.

5 CURSOR
HAT
SS
TRIGGER
60
RESET
10

GAMESEL
GAMEOP
GAMESE
OPTION
COMPUTER CONTR

75-309 IFET.

CAN THIS USE STD
STICK CONTROLS

5 + 52-53 + 5

53+10 ± 6

63

"KEYBOARD MUST BE SEXY" EWS

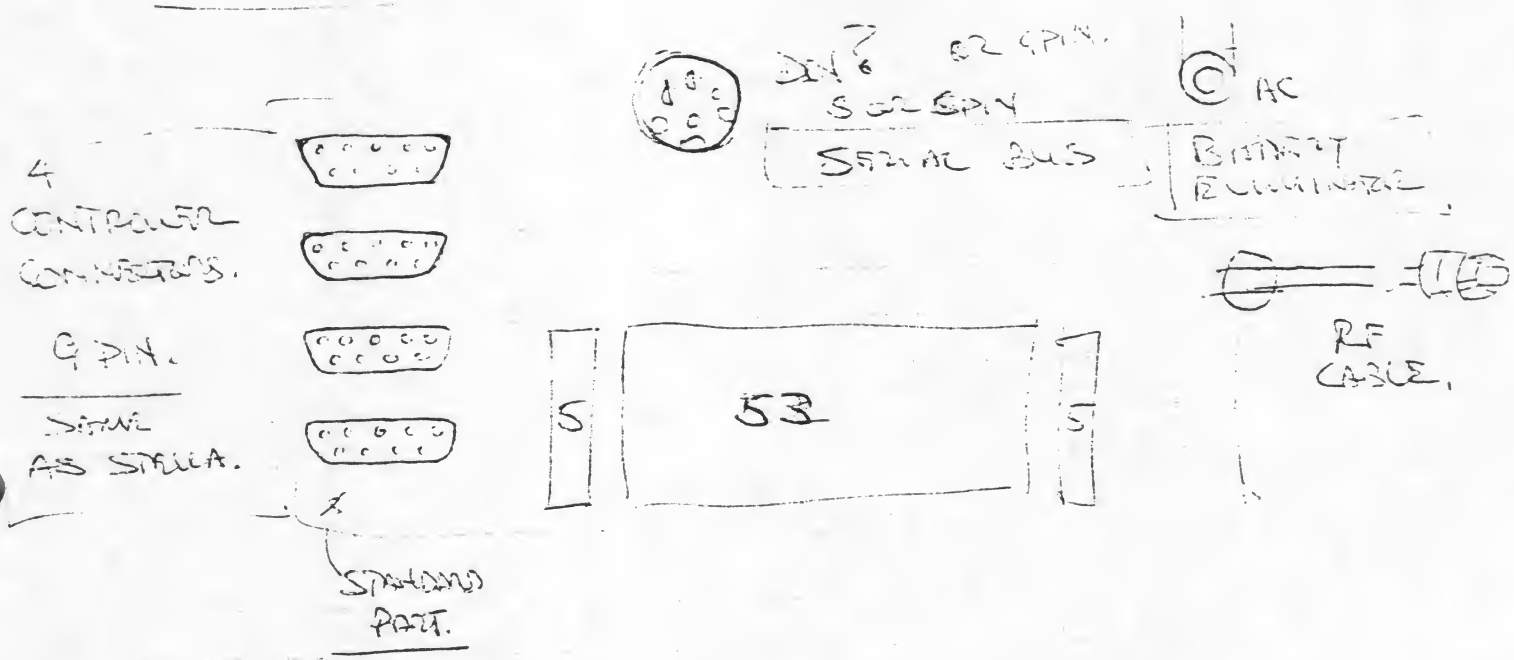
FANCY GAME PLAYER THAT
YOU CAN PLAY IT IN BASIC

WRITER DECKER	DATE 1-	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
COLLEEN.

JOHN ELLIS ACCOUNTS IDEA
OF PUTTING SIGNALS
FOR CASSETTE INTO CASSETTE.



CONFIDENTIAL

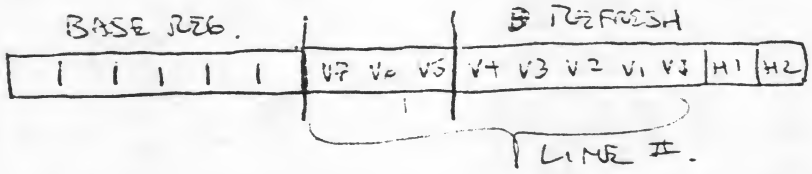
GAME OR PROJECT
ANTIC, TIA.

FOR AUTOMATIC OBJECT GENERATION:

TAKE REFRESH CYCLES.

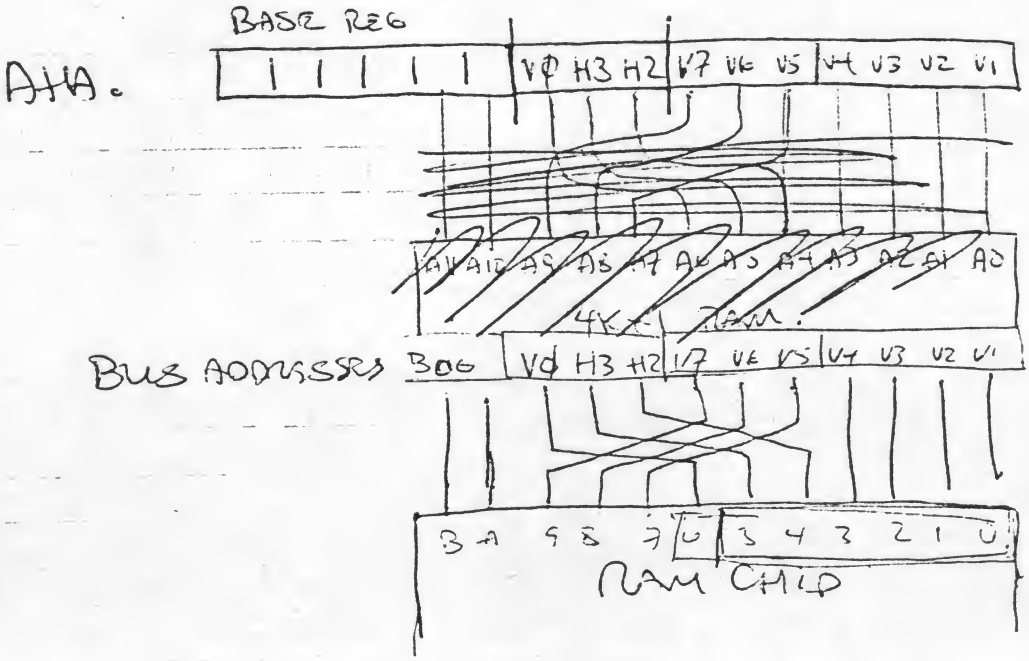
HAVE TIA RECOGNIZE THEM

ADD BASE POINTER TO REFRESH.



FOR FETCHING OBJECT GRAPHICS OUT OF MEMORY.

TIA CAN ACCEPT THOSE GRAPHICS



CONFIDENTIAL

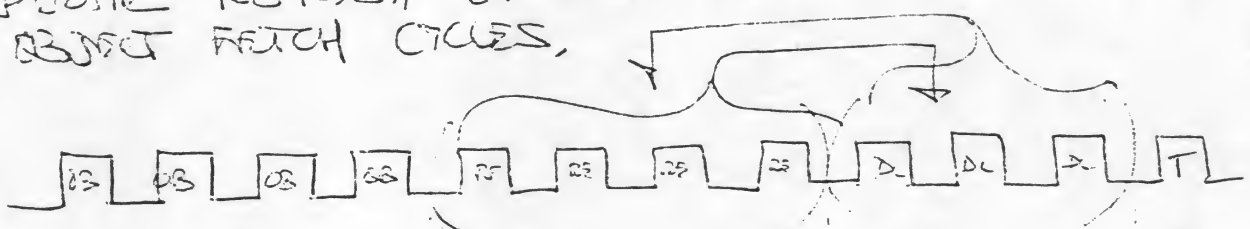
WRITER DECUIR	DATE	WITNESS	DATE

ATARI ENGINEERING LOG SHEET

GAME OR PROJECT
ANTIC / TIA2

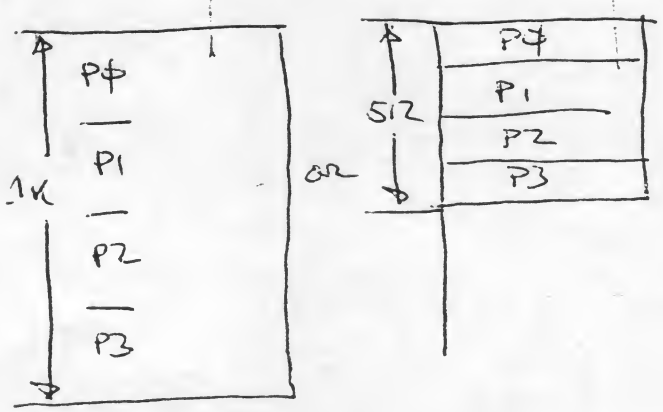
OBJECT GENERATOR

SEPERATE REFRESH CYCLES FROM OBJECT FETCH CYCLES.



AB 15	OBL 15	X	0	TL 15
14	OBL 14	X	0	TL 14
13	OBL 13	X	0	TL 13
12	OBL 12	X	0	TL 12
11	OBL 11	X	0	TL 11
10	OBL 10	X	1	TC 10
9	HB or OBL 9	X	DLC 9	TC 9
8	H2 or H3	X	DLC 8	TC 8
7	OBC 7 or H2	V5	DLC 7	TC 7
6	OBC 6	V4	DLC 6	TC 6
5	OBC 5	V3	DLC 5	TC 5
4	OBC 4	V2	DLC 4	TC 4
3	OBC 3	V1	DLC 3	TC 3
2	OBC 2	V0	DLC 2	TC 2
1	OBC 1	H3	DLC 1	TC 1
0	OBC 0	H2	DLC 0	TC 0

BUSES OF OBJECTS



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GAME OR PROJECT: TIA2 / ANTIC.

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VERTICAL $ DELAY. IN 128 BYTE TABLE

OBJECT DMA DATA.

LINE	P0 N	P1 N	P2 N	P3 N
2N	P0 N	P1 N	P2 N	P3 N
2N+1	P0 N+1	P1 N+1	P2 N+1	P3 N+1
2N+2	P0 N+1	P1 N+1	P2 N+1	P3 N+1
2N+3	P0 N+2	P1 N+2	P2 N+2	P3 N+2
2N+4	P0 N+2	P1 N+2	P2 N+2	P3 N+2
2N+5				

P0, P2 NOT DELAYED

P1, P3 DELAYED.

IF NOT DELAYED, CAPTURE OF 1ST LINE.
IF DELAYED, CAPTURE OF 2ND LINE.

REGISTERS IN ANTIC. FROM CPU POINT OF VIEW.

READ	BC	X
WRITE	OB3	X
WRITE	T COUNTER LOW.	
WRITE	T LATCH / TC HIGH	
R/W	TIMER (?)	
RSLD.	V COUNTER	
READ	STATUS.	
WRITE	NMI. TIMER CONTROL.	
WRITE		
WRITE	DLL	
WRITE	DLCH	

BASE ADDRESS CHARACTERS.
BASE ADDRESS OBJECTS.
MEMORY POINTER "T"

} READ VERTICAL COUNTER
INTERRUPT BITS. ETC.

HSCROLLING OFFSET
MODE (DMA)

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GAME OR PROJECT

TIA

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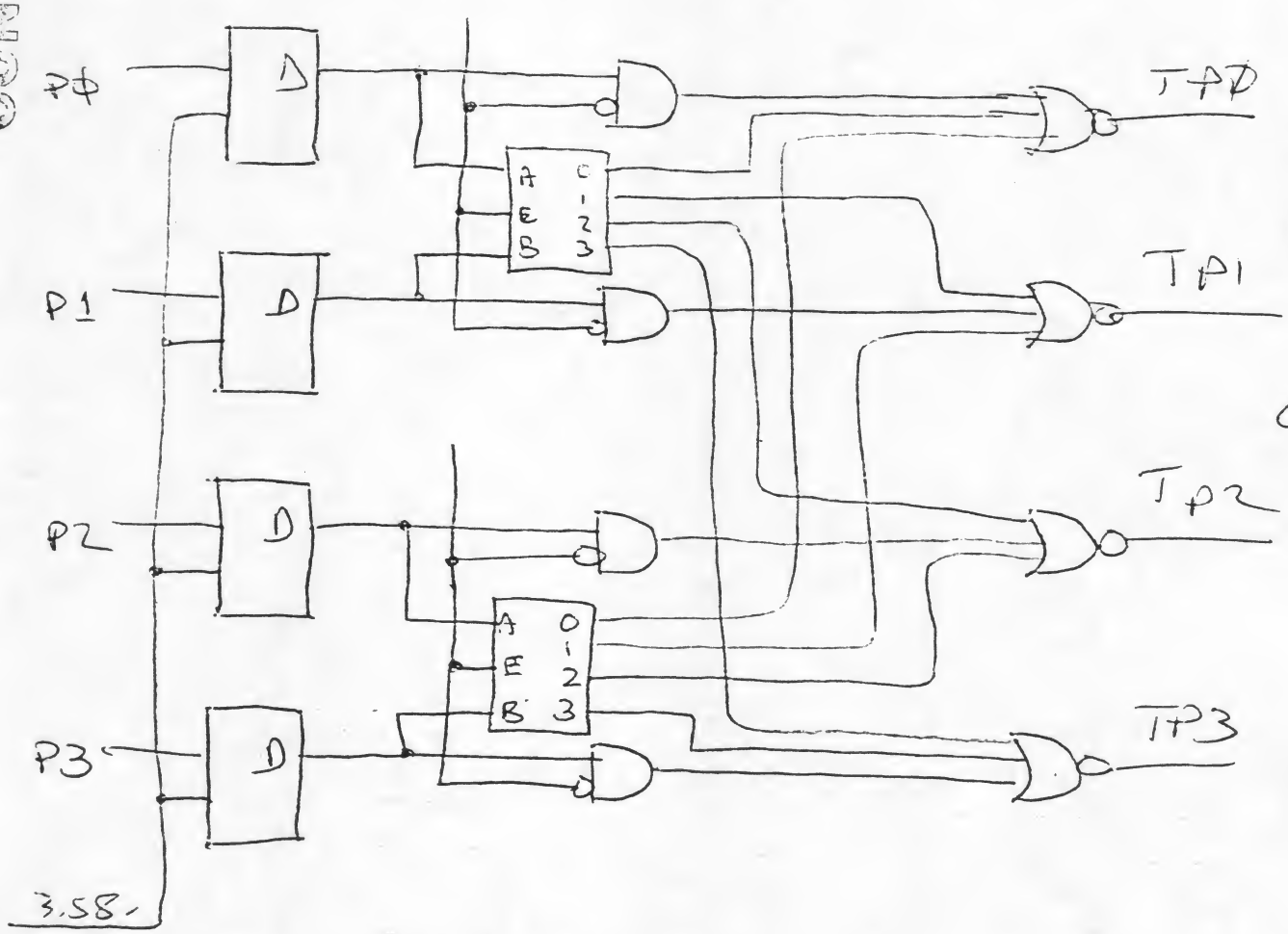
ANOTHER HOT IDEA.

GANG TWO 8 BIT TIA OBJECTS TO GETHER INTO ONE 4 COLOR/POINT OBJECT



EACH OBJECT CAN BE INDEPENDANT (ONE LEVEL)

OR PAIRED (TWO LEVEL)

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GAME OR PROJECT
CAILEY PADDLE MEETING

29 NOV 77

JOE WANTS TO DEFINE THE PRODUCT, AND GET IT OUT.

TWO CONTROLLERS.

SAM - QUERYS FROM ME.

6502	5.0
RAM 4K	12.8
ROM 4K	3.00
U A	3.0
ANTIC	6.00
TIA	7.50
POKEY	4.00
MISC	7.50
	40.80

KEYBOARD 64 @ $16 = (53+5+2)
32 @ $8

TOTAL PARTS $115.17
LABOR 12
COST TO BUILD. 127.17 ⇒ 300!!

"STUCK WITH THIS.

PROPOSED SOLUTIONS.

TWO PROPOSED PRODUCTS.

GAME PLAYER, NON EXPANDABLE = TOTAL PARTS

"CANDY" PARTS $85.50 NO KEYBOARD
+9 =$94.50 NO INTERFACE
ONE CONTROLLER CAPABILITY. SAME IC

BASIC STILL NOT FCC APPROVED

DESIGN BUT MAY NOT INTRODUCE

CAILEY + BUILT IN COLOR MONITOR

"ELIZABETH" $100 13" COLOR MONITOR

PARTS $211 +12 = $500

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GAME OR PROJECT
COLLEEN / CANDY / ELIZABETH

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ANY EFFORT TO BUILD SKILLS INTO IT?

JOE SEES THE TEST

FIC PROBLEM w/ COLLEEN
UC PROBLEM w/ ELIZABETH.

IF CHIP SET AVAILIBLE IN NOV 78
WE CAN SHOW IN JANUARY.

JOHN PURCH SUGGESTS
THAT JAPANESE MAY PUT
VIDEO INPUT ON FUTURE TV'S,

LOTS OF CHATTER...

PERHAPS

ADD SERIAL PORT TO CANDY
DELETE COLLEEN
BUILD ELIZABETH.

GAME OR PROJECT: COLLEEN & MADRO.

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SYNERGY MEMORY PRESENTATION

JACK BOURD
GEORGE REED
MARK ABSAR.

MEMORIES, PERIPHERALS & MICROS.

DO NOT GET INTO DYNAMIC RAMS

(USING POLYSILICON RESISTORS IN PLACE OF DEPLETION LOADS IN RAM CELLS.)
MOSTEK WAS IT, TOO

LOOKING ON HMOS.

16K STATIC !! 4K×4, or 2K×8
200 NSEC IS "SLOW"

JACK SAYS $3 EA 2114 IN 1979

70MA. 350 MW.

LOOKING FOR 4K×1S.

SOSG — COMPUTRON 1YR SOLOS.

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GAME OR PROJECT
PANDO - SYNERGY MEETING CONTINUES.

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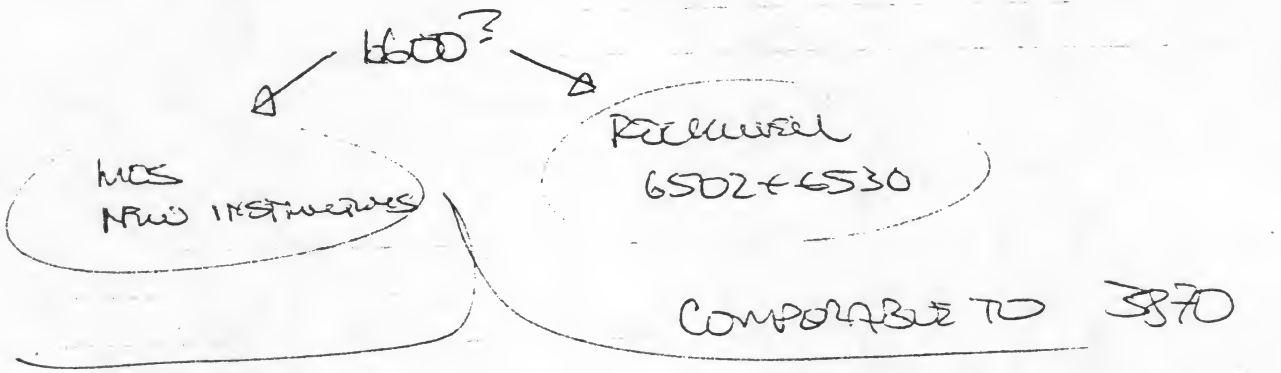
6551 - ACIA

6529

CRT CONTROLER

FLOPPY DISK CONTROLER

DID NOT AGREE ON 6600!!!



OUR DISCUSSIONS:

DESIGN FOR M6512
PUSH DEVELOPMENT OF 6519/09
MAKE DECISION LATER TO USE 6519 OR 12.

GAME OR PROJECT
PADDLE, SYNERGY

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6502 M6502 S6509

SOFTWARE COMPATIBLE

BC.
TALT.

UP AND SOURCE COMPATIBLE.

TSC
TALT.

HARDWARE COMPATIBLE,
NOT NECESSARY TO BE PIN OUT.

1ST PARTS ON M6502 END
1ST QUARTER.

QUESTIONS ASKED AND PARTIALLY ANSWERED

Q: WHAT IS REALLY IN CANDY FOR I/O?

(AL, STEVE, WILKERSON, JOHNSON) ANS:

COMPATIBLE W/STELLA IF IT DOESN'T COST EXTRA.

OPTIONAL KEYBOARD ~~AND/OR~~
AND CASSETTE INTERFACE — ACCESSED THRU CONTROLLER PORTS.
⇒ WIRE PORT PARALLEL TO VIA.

~~Q: DO ANY OF~~

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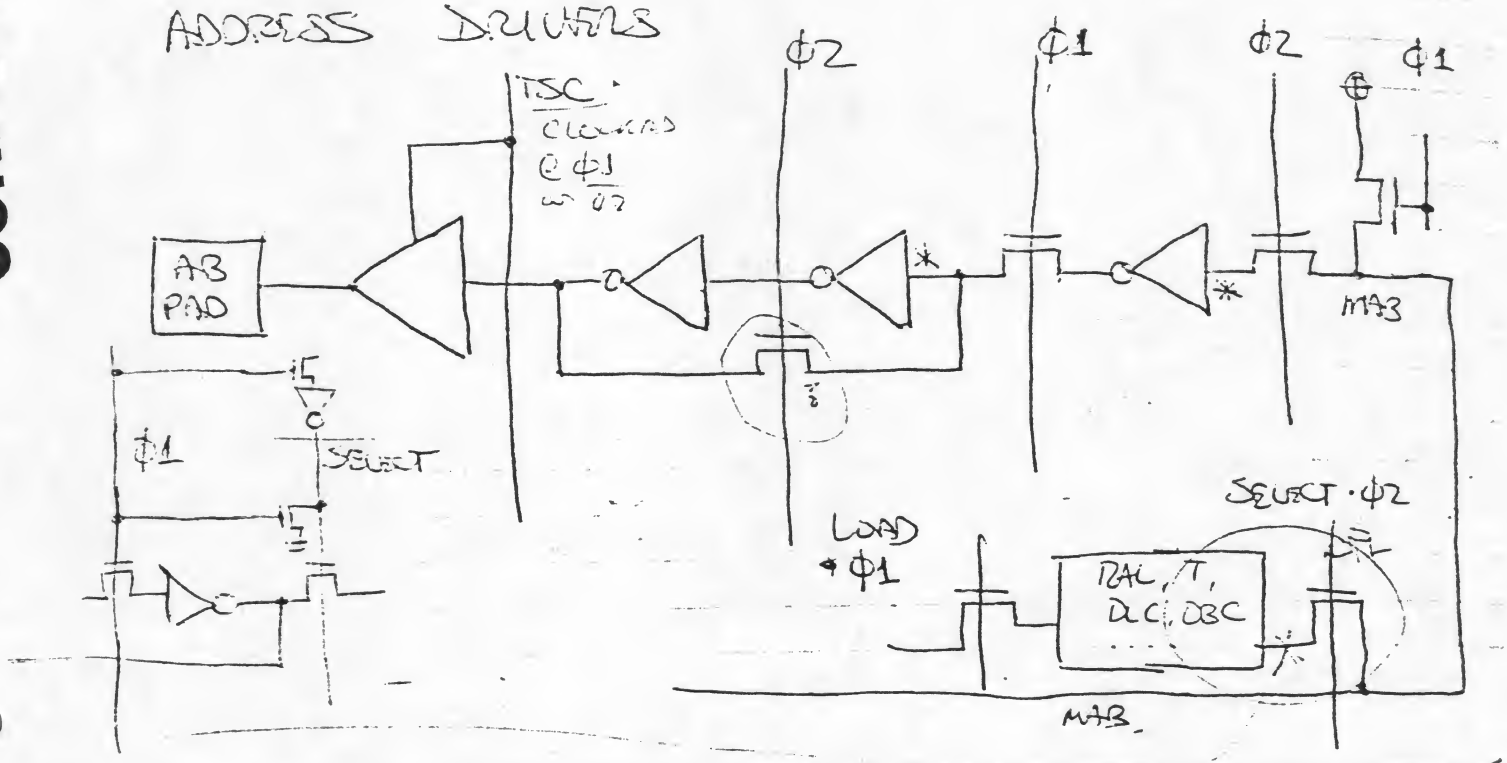
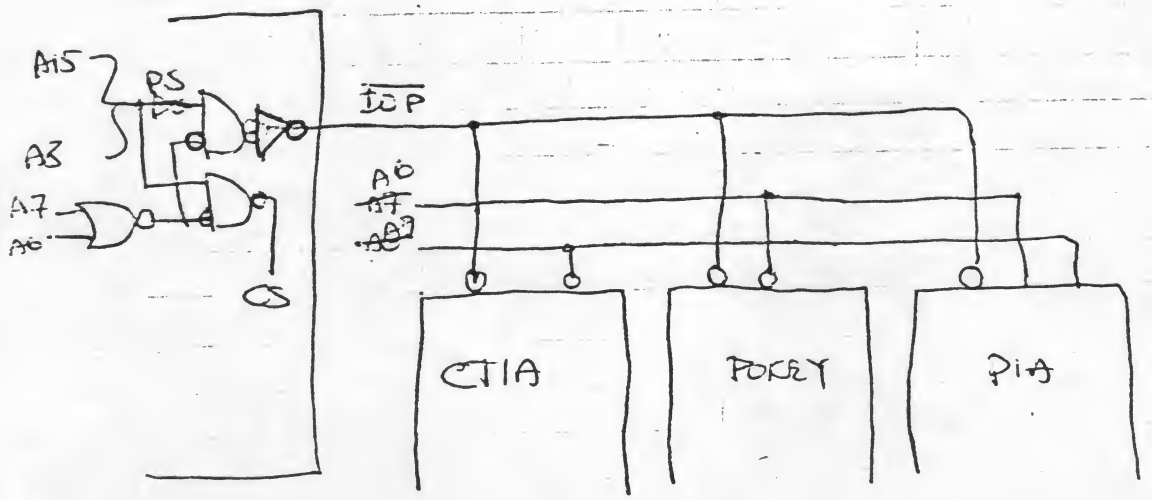
GAME OR PROJECT
ANTIC.

ADDRESS DRIVERS



CHIP SELECT SCHEME FOR COLLEEN/CANDY LSI



IOP	A7	A6	
1	0	0	ANTIC
0	0	1	POKEY
0	1	0	CTIA
0	1	1	PIA

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GAME OR PROJECT
COLORBAR/CANDY LSI PARTS

PINOUTS & INTERCONNECT.

SIGNAL	6509 (Base)		ANTIC		GTIA		POKEY		PIA 6520	
PACKAGE SIZE	Vss(2), Vcc	3	Vss, Vcc	2	Vss, Vcc	2	Vss, Vcc	2	Vss, Vcc	2
3.58 MHz			OSC	1	OSC	1				
ϕ_0	ϕ_{0IN}	1	ϕ_{0OUT}	1						
ϕ_1	ϕ_{1OUT}	1								
ϕ_2	ϕ_{2OUT}	1	ϕ_2	1	ϕ_2	1	ϕ_2	1	ϕ_2	1
$\overline{RES}$	$\overline{RES}$	1	$\overline{RES}$	1					$\overline{RES}$	1
$\overline{NMI}$	$\overline{NMI}_{IN}$	1	$\overline{NMI}_{OUT}$	1						
$\overline{IRQ}$	$\overline{IRQ}_{IN}$	1					$\overline{IRQ}_{OUT}$	1	$\overline{IRQA}, \overline{B}$	2
RDY	RDY IN	1			RDY_{OUT}	1				
$\overline{HALT}$	$\overline{HALT}_{IN}$	1	$\overline{HALT}_{OUT}$	1	$\overline{HALT}_{IN}$	1				
$\overline{DP}$			$\overline{IOPAGE}_{OUT}$	1	$\overline{CS\phi}$	1	$\overline{CS\phi}$	1	$\overline{CS2}$	1
R/W	R/W_{TS}	1	R/W_{TS}	1	R/W	1	R/W	1	R/W	1
SYNC	SYNC	1								
DB4-DB7	Dϕ-D7	8	D0-D7	8	D0-D7	8	Dϕ-D7	8	Dϕ-D7	8
AB4-AB5	Aϕ-A5	6	Aϕ-A5	6	Aϕ-A4	5	Aϕ-A3	4	RSϕ RS1	2
AB6	A6	1	A6	1			$\overline{CS1}$	1		1
AB7	A7	1	A7	1	$\overline{CS1}$	1				1
AB8-AB15	A8-A15	8		8						
VIDEO SYNC			$CSYNC_{OUT}$	1	$CBLANK_{OUT}$	1	$CBLANK_{OUT}$	1		
LUMA CODES			$AU\phi$-2 OUT	3	$AU\phi$-2 IN	3				
LUM			LUM40	1	Lumϕ-2	3				
CHROMA					CHR, DEL	2				
COLORS					CCOD ϕ-3	4				
AUDIO							AUDIO	1		
KEYBOARD							KSϕ-KS5, $\overline{KR1}$, 2	8		
SERIAL PORT							SCLK, SDIN, SDOUT	3		
POTS							POTϕ-7	8		
JOYSTICKS IN					IN ϕ-3	4				
JOYSTICKS DB									PAϕ-7, PB1-7	16
LIGHT PEN (CANDY PANELS)			$\overline{LPEN}$	1					CAϕ1, CBϕ1	4
OTHER	S.O $\frac{1}{2}$	1								
SPARE	nc	2	—		nc	1	—		—	
PINSTOTAL	40		40		40		40		40	

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GAME OR PROJECT
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MIKE ALBAUGH HAS CONVINCED

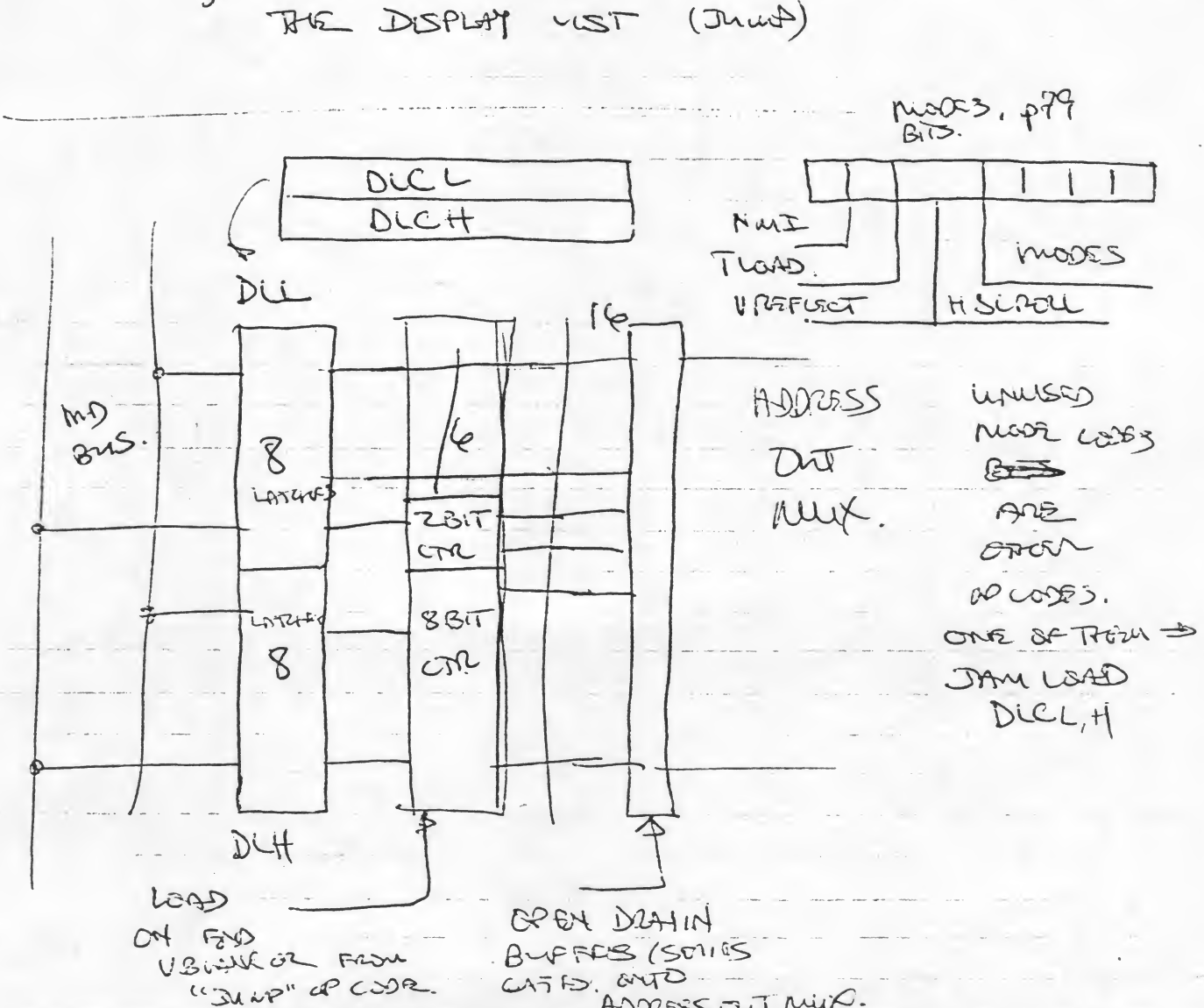
JAY AFTER LUNCH THAT THE

DISPLAY LIST COUNTER SHOULD

A) BE JAM LOADABLE

B) JAM LOAD REGISTER LOADED BY CPU.

C) JAM LOADABLE BY AN OP CODE IN THE DISPLAY LIST (JUMP)



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FROM LONG DISCUSSION OF VERTICAL SCROLLING

CONCLUSIONS FIRST

CPU CAN JAM LOAD Δ REGISTER

Δ REGISTER OR MODE PLA LOADED INTO Δ COUNTER.

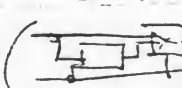
TWO STROBE LOCATIONS
- START SCROLL
  ΔCTR ← Δ REG INSTEAD OF MODE PLA
- END SCROLL
  MODE FETCH REQUEST SET AT ΔREG=ΔCTR INSTEAD OF ΔCTR=0

NMI FROM ANTIC SET AT SAME TIME AS MODE FETCH REQUEST (1 LINE AHEAD OF MODE FETCH)

HORIZONTAL SCROLLING.

SLIP COUNTER THAT IS SIDE LOADED ONCE/LINE - SCROLLS TO 1 COMPUTER CLOCK RESOLUTION - USED TO GENERATE T COUNTER AND GRAPHICS DMA FETCHES.

½ COMPUTER CLOCK (1 COLOR CLOCK) SCROLLING DONE WITH SIMPLE 2:1 MUX AT OUTPUT OF MODE/GRAPHICS PLA - JUST BEFORE ANTIC OUTPUT



WRITER JOE DECUIR	DATE 12 DEC 77	WITNESS	DATE

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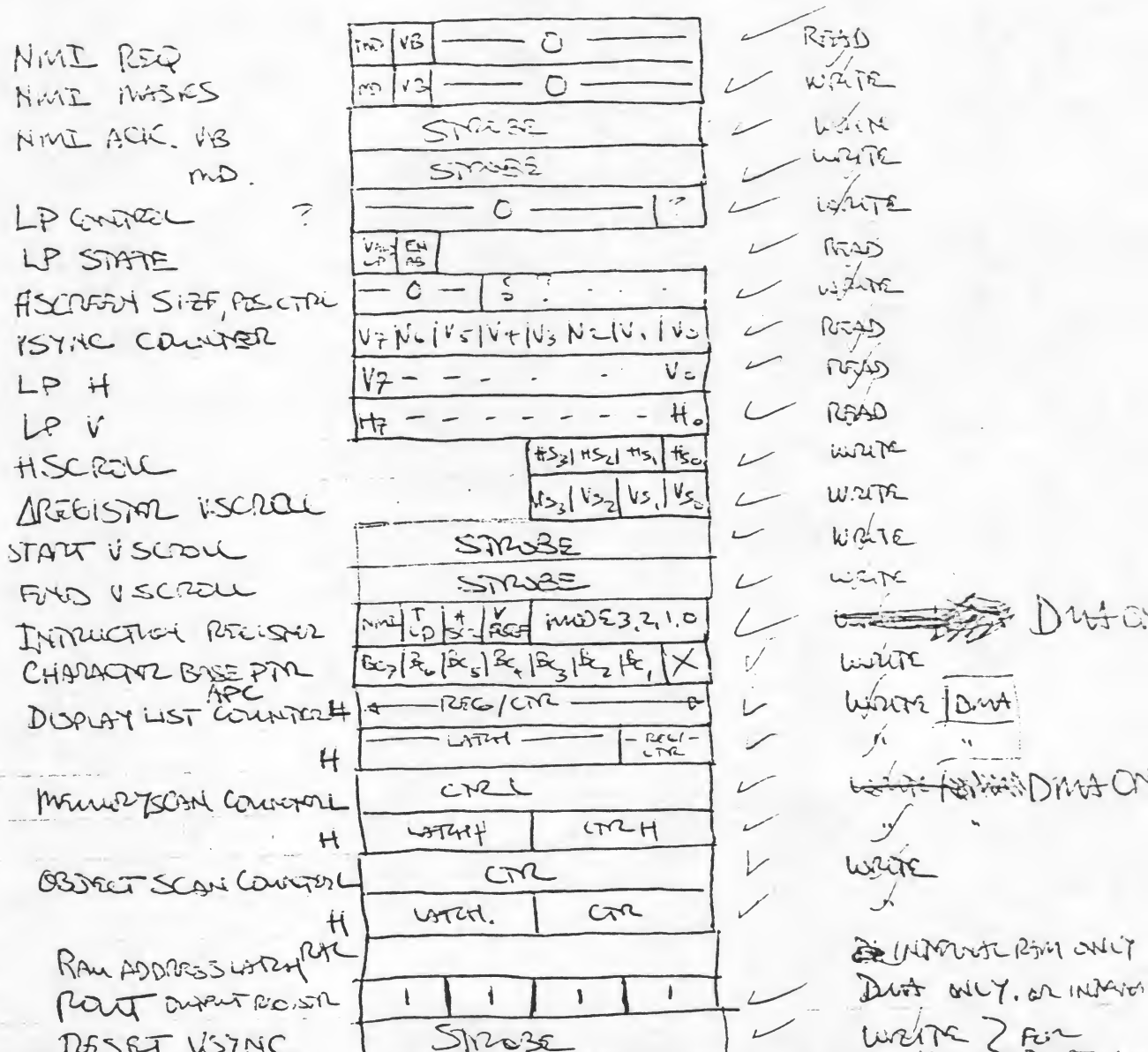
INVENTORY of REGISTERS.


NMI REQ
NMI MASKS
NMI ACK. VB
DLI
LP CONTROL
LP STATE
HSCROLL
VSYNC COUNTER
LP H
LP V
HSCROLL
VREGISTER VSCROLL
START VSCROLL
END VSCROLL
INSTRUCTION REGISTER
CHARACTER BASE PTR
DISPLAY LIST COUNTER
MEMORYSCAN COUNTER
OBJECT SCAN COUNTER
RAM ADDRESS LATCH
PORT OUTPUT REGISTER
RESET VSYNC
RESET HSYNC.
OBJECT SCAN ENABLE
READ
WRITE
STROBE
DMA CTL
DMA
APC
REG/CTR
LATCH
CTR
CTR H
CTR L
LATCH.
WRITE
WRITE
WRITE

GAME OR PROJECT: ANTIC

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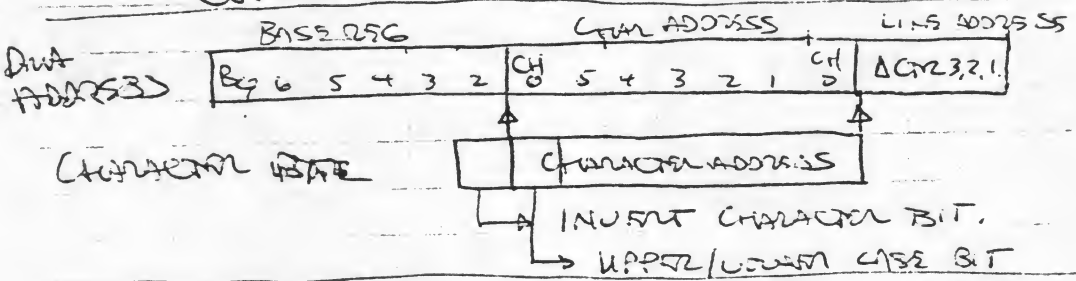
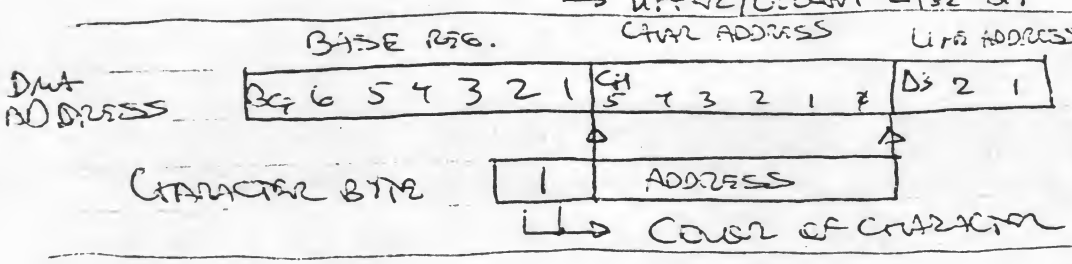
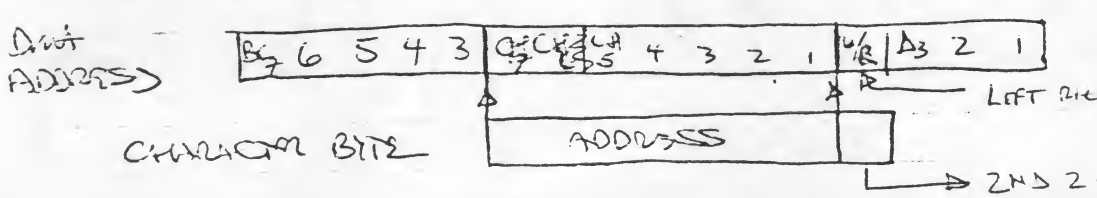
INVENTORY of MODE CODES. (FROM P85)

0000	BLANK (BACKGROUND) (3 BIT N) (1-8)		CTR
0001	JUMP 1 LINE BACKGROUND AND RELOAD		DISP. LIST
0010	(40 CH UPPER CASE)		?
0011	40 CH UPPER AND LOWER CASE		?
0100	20 CH x 5 COLOR x 8 LINES		20 + 20 DMA/LINE
0101	20 CH x 5 COLOR x 8x2 LINES		
0110	20 CH x 4 COLOR x 8 LINES		
0111	20 CH x 4 COLOR x 8x2 LINES		
~~(40 CELL x 2 COLOR x 8 LINES)~~			DELETED
1000	40 CELL x 4 COLOR x 8 LINES		10 DMA / LINE
1001	80 CELL x 2 COLOR x 4 LINES		
1010	80 CELL x 4 COLOR x 4 LINES		20 DMA/LINE
1011	160 CELL x 2 COLOR x 2 LINES		
1100	160 CELL x 4 COLOR x 2 LINES		40 DMA/LINE
1101	320 CELL x 2 LEVEL x 1 LINE		

CHARACTER ADDRESS FORMATS:







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GAME OR PROJECT
COLLEEN / CANDY.

INTERRUPT STRUCTURE

RESET — ONLY POWER ON —
ALSO ENTERED BY BREAK KEY.

NMI — VIDEO INTERRUPTS.
(MASKABLE WITHIN ANTIC)
1. VBLANK — START VBLANK
2. DISPLAY BLOCKS — END DISPLAY BLOCK

IRQ — NON VIDEO I/O
(MASKABLE ON CHIP AND IN SOURCE)
1. KEYBOARD — FOUND KEY, BREAK KEY
2. SERIAL PORT — INPUT BYTE, SENT BYTE
3. AUDIO TIMER. — END COUNT.
4. EXTERNAL DEVICES ON EXPANSION BOX.
??

LIGHT PEN I/O NOT INTERRUPT DRIVEN,
TRIGGER PORTS NOT INTERRUPT DRIVEN
JOYSTICKS NOT INTERRUPT DRIVEN
POTS NOT INTERRUPT DRIVEN

ANTIC — MOSTLY DMA
DA — POSSIBLY DMA

JAY'S SUGGESTION — 14 DEC 77

BRING IN EXTERNAL EXPANSION INTERRUPT VIA ONE OF CA1,2, CB1,2 PORTS,

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GAME OR PROJECT
POKEY SERIAL PORT DISCUSSION W/MIKE

110, 300
1200, ~~2400~~, 4800
9600, 19200

MIKE SUGGEST 16X CLOCK

DOESNOT JUST TALK TO OTHER ATARI PRODUCTS.

MIKE RAISES ISSUES ABOUT

CLOCK TOLERANCE - SKEWING
IF BUFFERS ARE NOT REGENERATIVE - SYNCHRONOUS WITH CLOCK.

NEVER HAVE MORE THAN ONE BAUD RATE OUT THERE AT ANY ONE TIME.

PERHAPS THE CLOCK SHOULD BE BIDIRECTIONAL.

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ANTIC.

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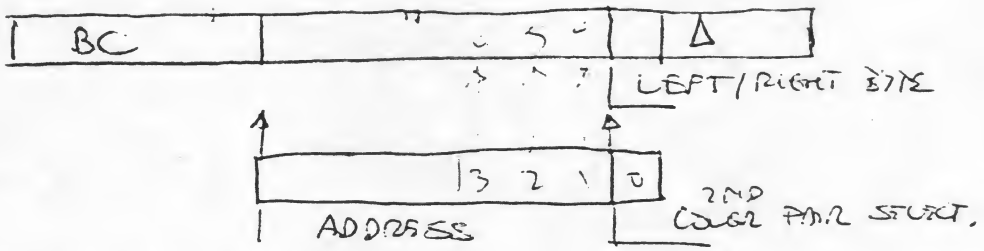
SCOTT'S SUGGESTION:

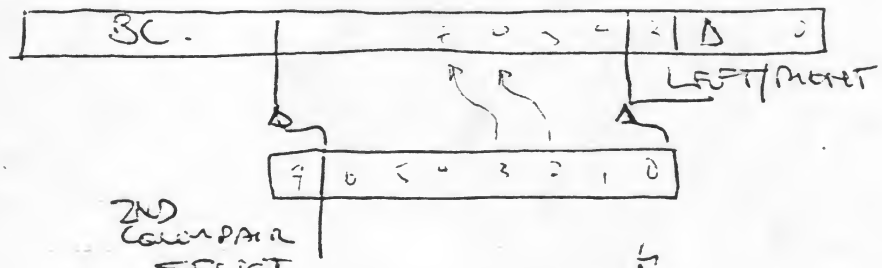
IN 20 CHARACTER x 4 COLOR,

SHIFT CHARACTER UP

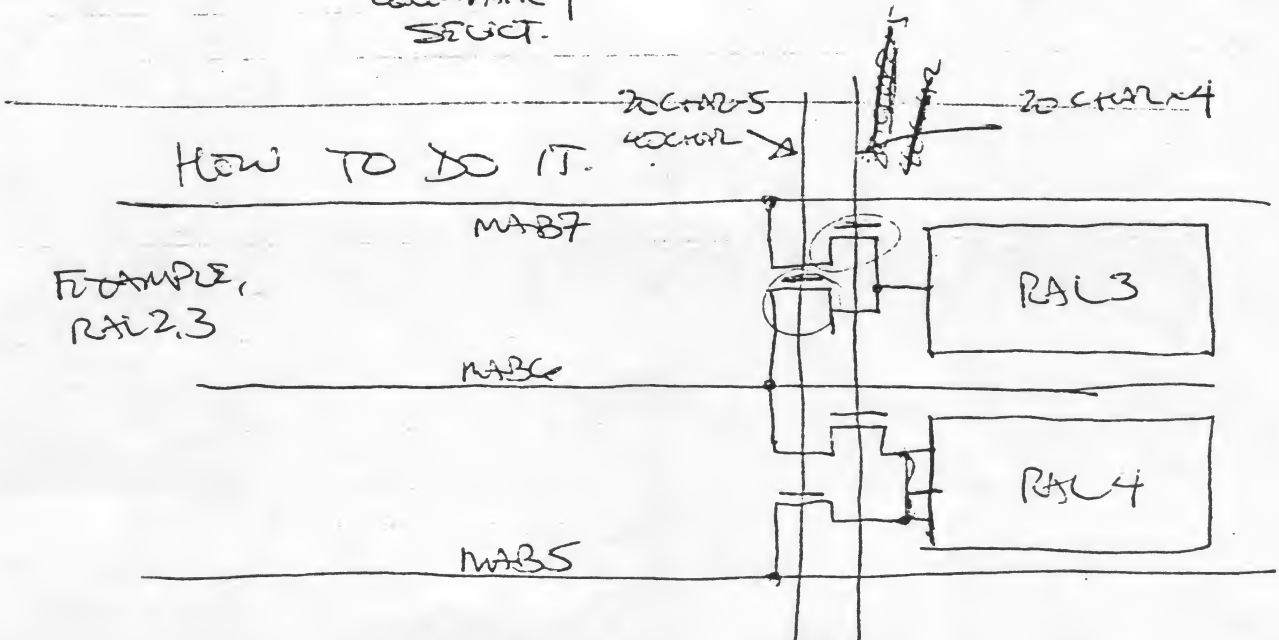
INSTEAD OF



SHIFT CONTENTS UP.



HOW TO DO IT.



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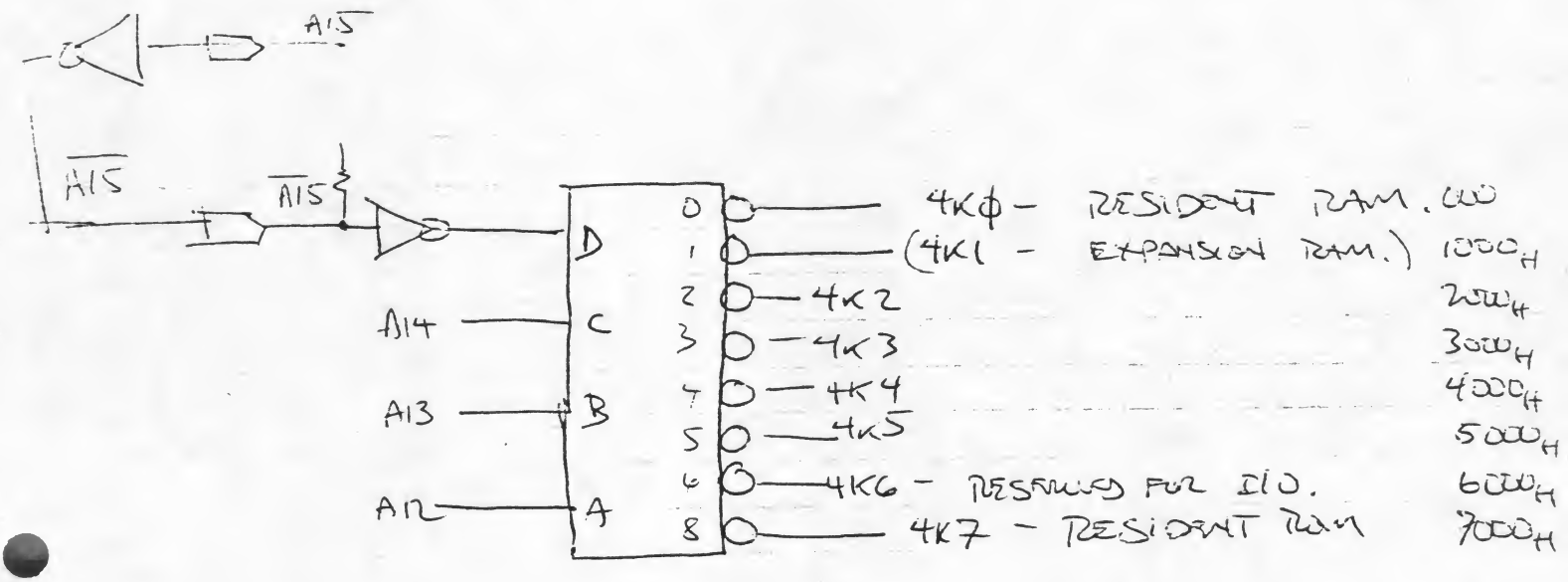
GAME OR PROJECT
COLECO CANDY

SUGGESTED ADDRESS DECODING SCHEME



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GAME OR PROJECT

ANTIC CHIP. DMA TIMING

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6 DMA SEQUENCES.

1. 40 CELL/4COLOR, 80 CELL/2COLOR.

   10 DMA/LINE. 1ST LINE ONLY

   LEADS BY 4 CYCLES
   4 CYCLES TOTAL
   3 CYCLES FROM

2. 80 CELL/4COLOR, 160 CELL/2COLOR

   20 DMA/LINE 1ST LINE ONLY

   LEADS BY 4 CYCLES
   4 CYCLES TOTAL
   4 CYCLES FROM

3. 160 CELL/4COLOR

   40 DMA/LINE 1ST LINE ONLY.

   LEADS BY 4 CYCLES
   4 CYCLES TOTAL
   2 CYCLES FROM

4. 20 CHARACTER/5COLOR

   20 +20 DMA 1ST LINE
   20 DMA/LINE THEREAFTER

   LEADS BY 6 CYCLES
   6 CYCLES TOTAL
   4 CYCLES FROM

5. 20 CHARACTER/4COLOR

   20 +40 DMA 1ST LINE
   40 DMA/LINE THEREAFTER

   LEADS BY 8 CYCLES
   8 CYCLES TOTAL
   4 CYCLES FROM

6. 40 CHARACTER/2COLOR
   40 DMA 1ST LINE
   40 DMA/LINE THEREAFTER

   LEADS BY 6 CYCLES
   6 CYCLES TOTAL
   2 CYCLES FROM

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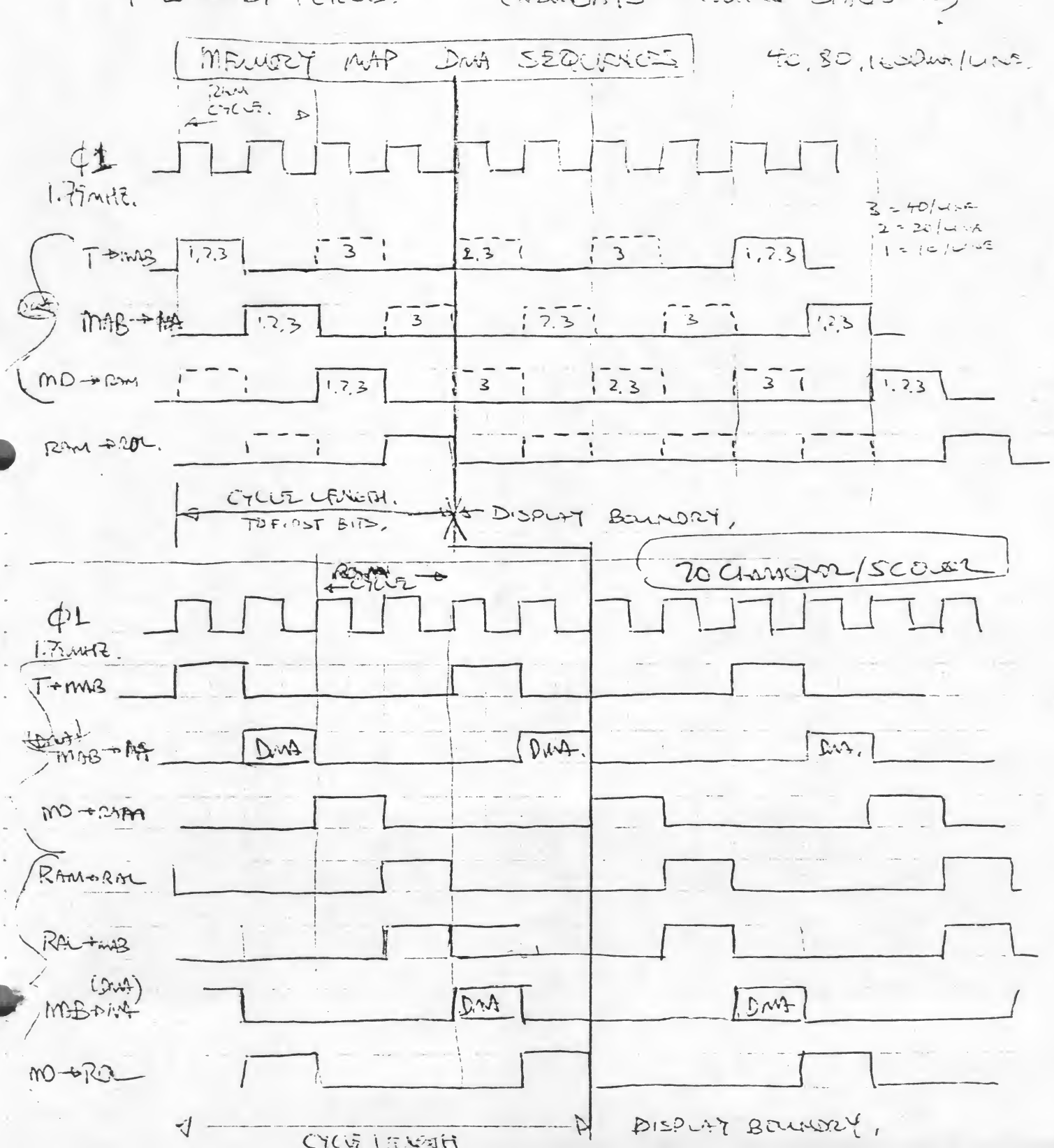
GAME OR PROJECT

ANTIC CHIP DMA TIMING

T LEADS BY 4 CYCLES. (FROM JAYS TIMING DIAGRAMS)



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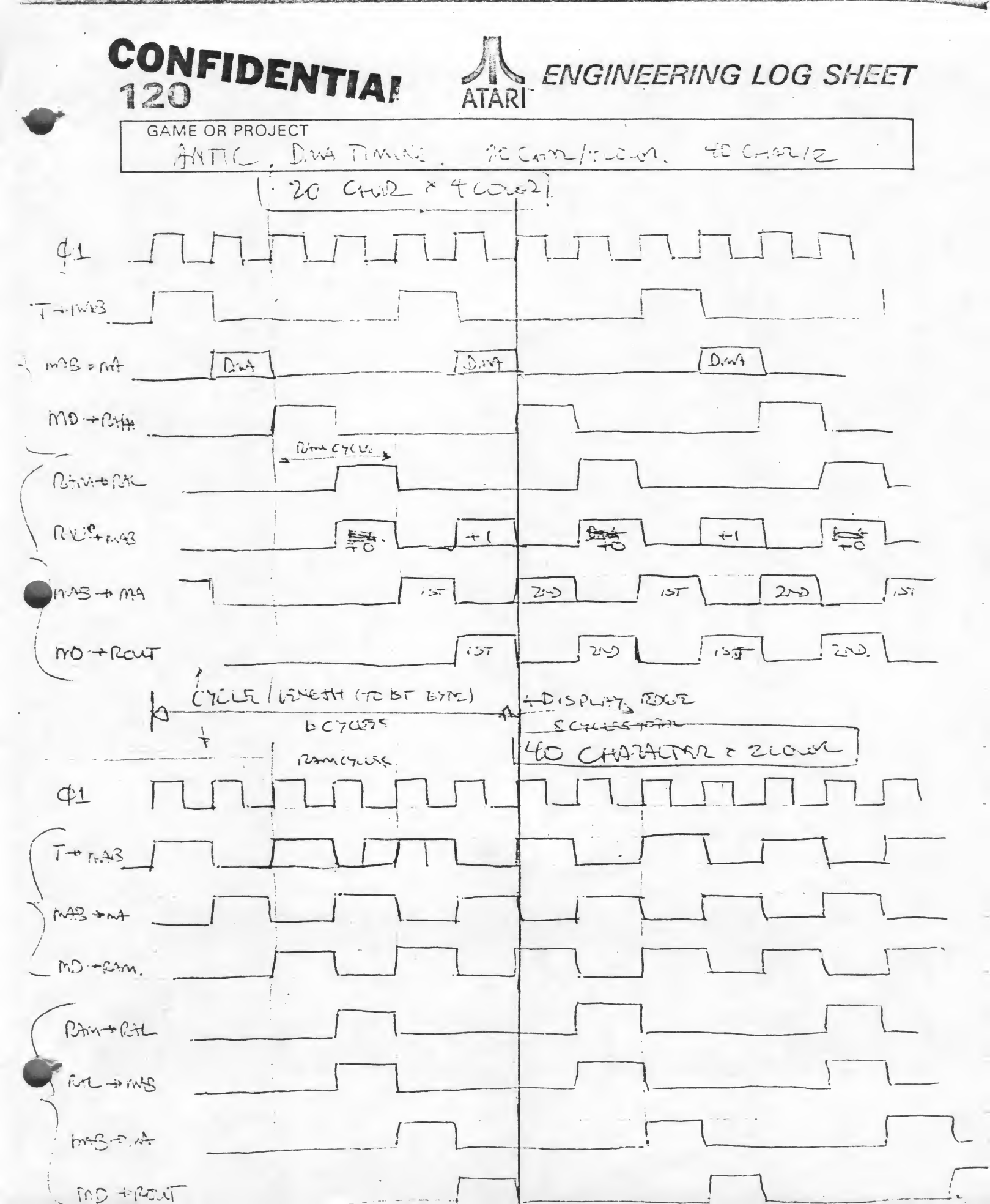
GAME OR PROJECT

ANTIC. DMA TIMING. 20 CHAR/1 LOW. 40 CHAR/2



ET

SUE ORTH.

DESIGN of
Man Computer DIALOGUES

JAMES MARTIN

PRENTICE HALL

17.50

ENGLEWOOD CLIFFS N.J.

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